

# DAQ523

MTCA.4 Data Acquisition Sub-system,  
12-channel 16-bit @ 125 MSPS



AMC523



MRT523

## Key Features

- Complete Data Acquisition sub-system
- Supported by DAQ Series™ data acquisition software
- Twelve channel ADC 16-bit @ 125 MSPS using AD9653
- Dual DAC 16-bit @ 250 MSPS using MAX5878
- Xilinx Kintex-7 FPGA XC7K410T with 2 GB of DDR3 memory
- Trig in/out configurable by software (external trigger via front or Port 17)
- Double module, mid-size (full-size optional) AMC and RTM, compliant to MTCA.4
- Internal or external clock, Trig in/out configurable by software

## Benefits

- Complete integrated solution with EPICS support and example GUI
- High performance ADC/DAC sub-system with Kintex-7 FPGA
- Comprehensive driver support
- Customizable analog front end
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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# DAQ523

The DAQ523 is a digitizer sub-system in MTCA.4 form factor, comprising an FPGA AMC, an ADC rear transition module, and full software/firmware complete with DMA engine and EPICS support. The equipment can be operated from a simple user-level API, via a development API, or via EPICS. The user interface is consistent with other VadaTech data acquisition products.

The high sample rate, 16-bit digitization and MTCA.4 form factor makes this sub-system ideal for research and industrial applications. The dual channel DAC, driven from the onboard Kintex FPGA can be used to implement low-latency feedback for Hardware in the Loop (HWIL) test applications.

An RS-232 Port is also available from the FPGA if the customer desires to implement a soft-processor in the FPGA and utilize a serial console, and quad SFP+ Ports are available on the front panel (these require user firmware development).

The MRT523 is capable of accepting user-designed mezzanine modules for sensor input direct to the chassis. This allows users to match the analog front end to specific project requirements. Contact VadaTech sales for details.

## AMC523 – Dual DAC 16-bit @ 250 MSPS, Kintex-7, MTCA.4

The AMC523 in an MTCA.4 compliant module providing a Kintex-7 with digital I/O, onboard Flash memory and 2 GB of DDR3. The FPGA accepts input, via the RTM connector, from the ADCs on a mating MRT523. The module also includes dual DAC, 16-bit @ up to 250 MSPS using MAX5878, with the outputs routed to the RTM.

The FPGA is reconfigurable by the user to support various fabrics over Ports 4-11 (PCIe being the default for use with the DAQ-Series software provided).

The AMC523 allows for flexible external or internal clocking. The module has a Trig In/Out signal that can be sourced from the front panel or TCLKA-D.

The FPGA interfaces to the front panel via quad SFP+, I/O headers, JTAG, CLK In/Trig In/Out, and LEDs.

**Note:** The SFP+ interfaces are not currently supported by the DAQ-Series software and require user code development if they are to be used.

An RS-232 Port is also available from the FPGA if the customer desires to implement a soft-processor in the FPGA and utilize a serial console.



Figure 1: AMC523

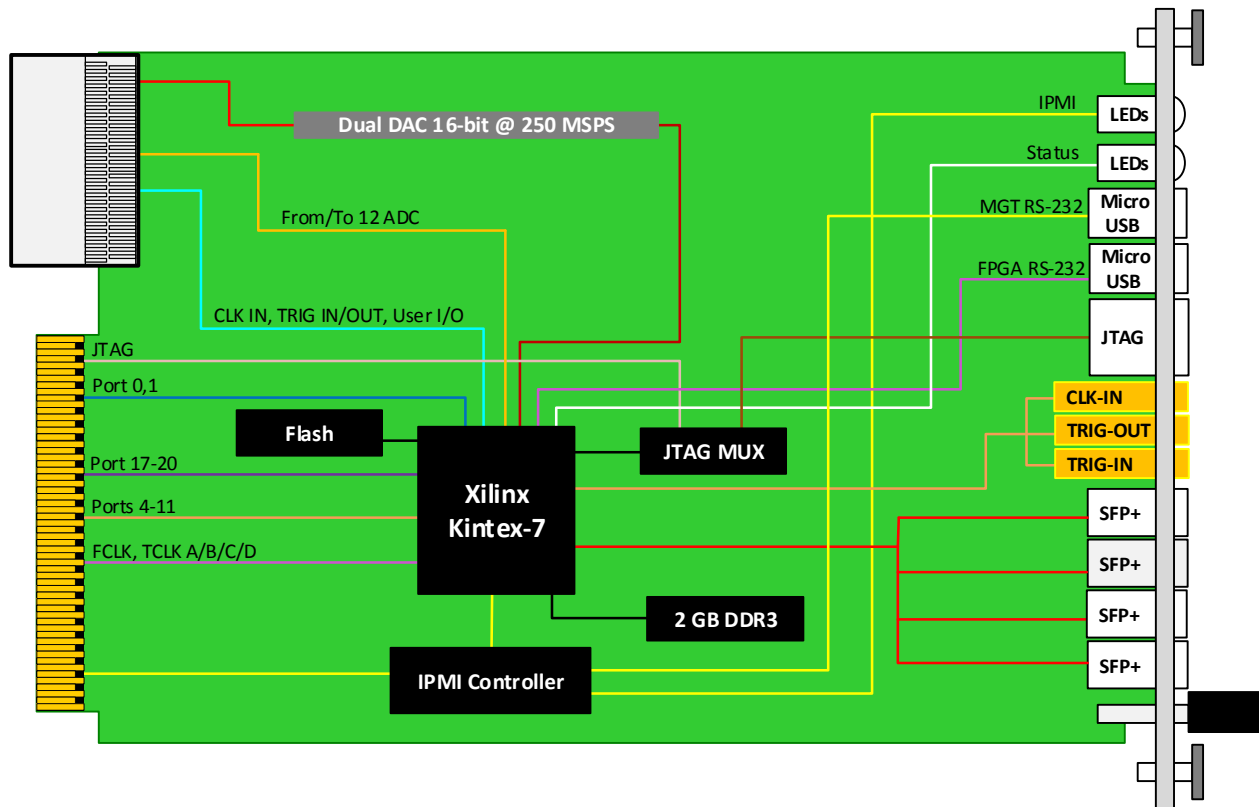


Figure 2: AMC523 Functional Block Diagram

## MRT523 – MTCA.4 RTM for AMC523, 12 Ch ADC

The MRT523 is an MTCA.4 compliant MicroRTM providing 12 channels of ADC, 16-bit at up to 125 MSPS utilizing AD9653 devices. It also routes the dual DAC outputs of the AMC523 to rear panel connectors via a mezzanine board. The ADC inputs are routed directly to the AD9653s to provide high performance without signal degradation, so input signals should be limited to +/-1V (either by the user or by selection of an appropriate mezzanine card).

A 1 Mb EEPROM is provided associated with each AD9653, accessible by an I2C bus from the FPGA on the mating AMC523. This can be used store calibration data for correcting for integral non-linearity, offset and gain errors, etc., to optimize DAQ performance.

The MRT523 accepts a mezzanine card that accepts electrical or optical analog inputs from the rear panel, provides signal conditioning as required, and provides +/-1V signals to the MRT. Additionally, the MRT523 routes digital I/O to the mezzanine, including a local I2C bus that can be used for functions such as a gain/offset control. A cut-out in the rear panel allows I/O connector choice to be made by the mezzanine designer, with the mezzanine routing signals to the MRT via flex way connectors for ease of integration.



Figure 3: MRT523

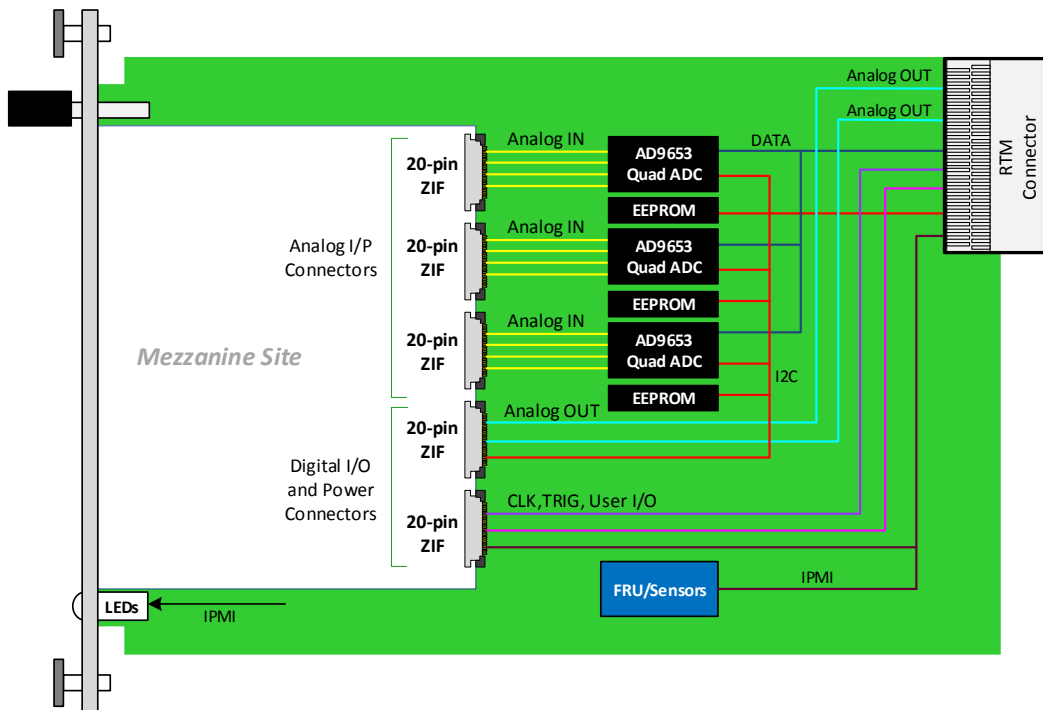


Figure 4: MRT523 Functional Block Diagram (Sold Separately)

## MZ523X – ANALOG INPUT MEZZANINE

The MRT523 accepts various VadaTech mezzanine modules (MZ523x series), allowing the user to select functionality according to their project requirements. In addition, users can implement their own mezzanine designs to a published interface specification from VadaTech, allowing them to support special-to-type interfaces or specific input filtering requirements.

Refer to [MRT523 Datasheet](#) and Mezzanine card datasheets (MZ523x for VadaTech versions) for available I/O channels and signal conditioning options. If you are using a custom or third-party mezzanine, ensure that the analog inputs are within +/-1V.

# Data Acquisition

VadaTech offers a wide range of FPGA AMCs, RTMs, FMC Carriers and FMCs that can be combined to build a Data Acquisition (DAQ) sub-system. The DAQ Series software, when used with a supported hardware configuration, provides all that is needed to configure the system, acquire data and transfer it to a host processor. It also includes a user-configurable Graphical User Interface (Figure 5), which incorporates real-time display of acquired data. The host can be within the MTCA system or, via PCI113 or PCI123, in a separate PC. Full documentation is provided to allow users to customize system behavior or develop their own application on the AMC/FMC hardware.

The DAQ includes data acquisition software that allows users to get up and running quickly and easily, while providing a high level of performance and allowing the user to extend functionality by adding their own FPGA code. Please contact VadaTech sales for the latest information on supported combinations of VadaTech hardware. (Note that the DAQ Series software is not currently supported for 3rd party hardware).

Components provided in the DAQ software include:

- System libraries to configure clocking and triggers
- Sequencer to configure the acquisition (duration, start, stop)
- High-performance DMA firmware for acquiring ADC outputs and transferring to host processor
- Linux driver for host processor (e.g. AMC72x)
- EPICS channel access client API
- Pre-configured GUI (based on Qt Creator)

This software set allows the user to acquire, transfer and display data without the need for any user programming of the hardware. Status information is included in the GUI display, to ease integration and debugging activity.

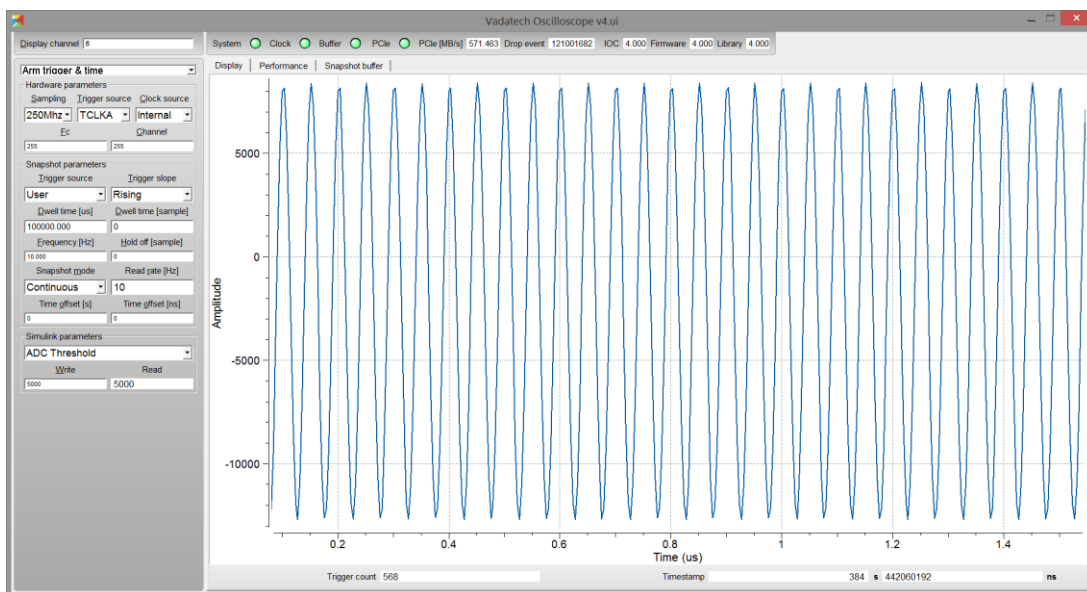


Figure 5: Typical Graphic User Interface Display

The data acquisition software provided as part of the DAQ can be used as-delivered without the user needing to develop any FPGA code.

Full source code is provided for the libraries, sequencer, DMA, Linux driver and GUI, allowing users to easily customize or brand to their own requirements at the exception of a low level PCIe IP from Xilinx provided only as Netlist (this low-level block doesn't require modification/customization from integrators or end-users).

# Configuration and Functionality

The DAQ523 comprises of an AMC523 (Kintex-7 FPGA with dual DAC), an MRT523 (12-channel ADC) with optional mezzanine and software to configure the system, acquire data and transfer it to a host processor. The host can be within the MTCA.4 system or, via PCI113 or PCI123, in a separate PC. DAQ Series software is provided via VadaTech download center, and full documentation is provided to allow users to customize system behavior or develop their own application on the AMC/MRT523 hardware.

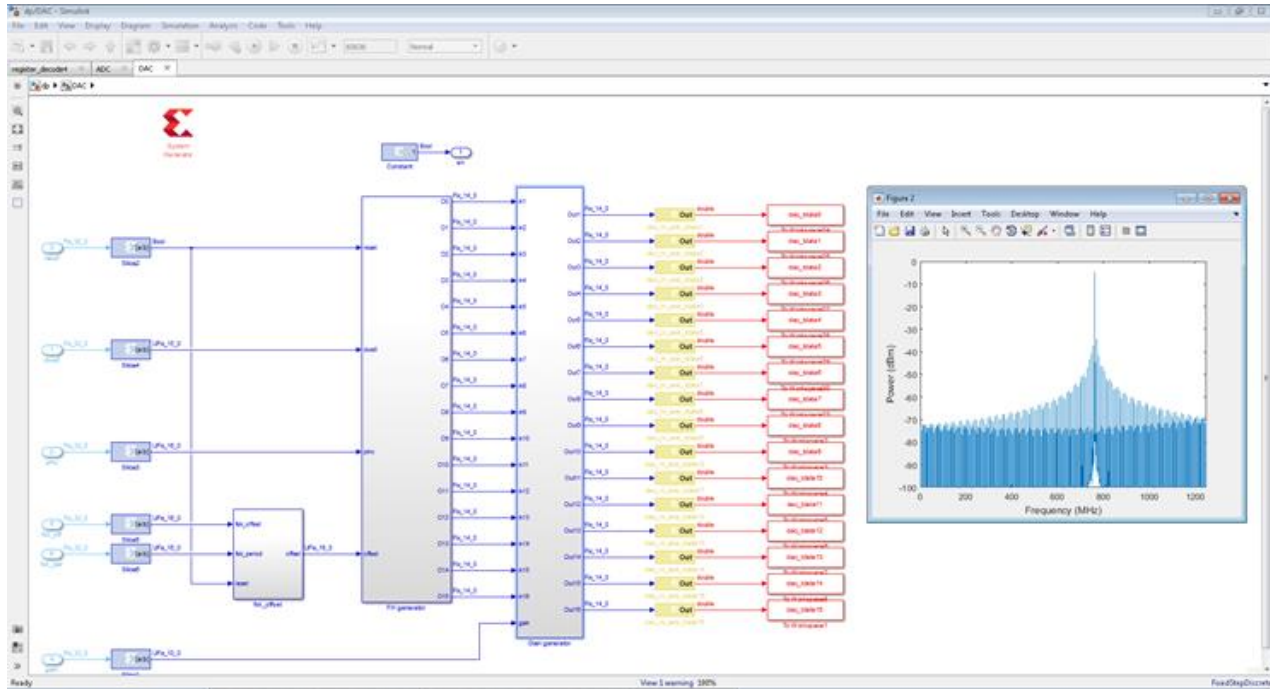


Figure 6: Example of DAQ Signal Processing

# Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from customer support site along with the reference images.

## Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

[Xilinx Vivado Design Suite](#), [Xilinx System Generator for DSP](#).

# Specifications

Architecture			
<b>Physical</b>	<b>Dimensions</b>	Double module, mid-size (full-size optional)	
	<b>AMC</b>	FPGA Carrier, 2 DAC	
	<b>RTM</b>	12 ADC input and routes 2 DAC outputs	
	<b>Resolution</b>	16-bit resolution per port	
	<b>CLK/TRIG</b>	Internal/External clock with TRIG IN/OUT	
	<b>Memory</b>	2 GB of DDR3, Flash	
Standards			
<b>MTCA</b>	<b>Type</b>	MTCA.4 with RTM support	
<b>AMC</b>	<b>Type</b>	AMC.1 and AMC.2	
<b>Module Management</b>	<b>IPMI</b>	IPMI v2.0	
<b>PCIe</b>	<b>Lanes</b>	Dual x4 or single x8 via FPGA to AMC	
<b>Ethernet</b>	<b>GbE</b>	1000-BaseBX	
Configuration			
<b>Power</b>	<b>DAQ523</b>	~15W application specific (up to 40W)	
<b>Environmental</b>	<b>Temperature</b>	See <a href="#">Ordering Options</a> Storage Temperature: -40° to +85°C	
	<b>Vibration</b>	Operating 9.8 m/s <sup>2</sup> (1G), 5 to 500 Hz on each axis	
	<b>Shock</b>	Operating 30Gs on each axis	
	<b>Relative Humidity</b>	5 to 95% non-condensing	
	<b>Front Panel</b>	<b>Interface Connectors</b>	Micro USBs for MGT RS-232 and FPGA RS-232 FPGA JTAG port TRIG In/Out, Clock In 4 SFP+
<b>LEDs</b>		IPMI management control, FPGA 8 user defined LEDs	
<b>Mechanical</b>		Hot swap ejector handle	
<b>Software Support</b>		<b>Operating System</b>	Linux and Scientific Linux
Other			
<b>MTBF</b>	MIL Hand book 217-F@ TBD hrs		
<b>Certifications</b>	Designed to meet FCC, CE and UL certifications, where applicable		
<b>Standards</b>	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards		
<b>Warranty</b>	Two (2) years, see <a href="#">VadaTech Terms and Conditions</a>		

## INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.



# Ordering Options

## DAQ523 – A0C-DEF-G0J

<b>A = Mezzanine (MRT523)*</b> 0 = MZ523A (Passive pass through) 1 = MZ523B (Programmable gain) 2 = No mezzanine fitted 3 = MZ523C (Optical detector) 4 = Reserved 5 = Reserved	<b>D = FPGA (AMC523)</b> 1 = Reserved 2 = Reserved 3 = Reserved 4 = XC7K410T 5 = Reserved	<b>G = SFP+ TXCVRS (AMC523)</b> 0 = No TXCVRS 1 = GbE LC/SX (850 nm) 2 = GbE LC/LX (1310 nm) 3 = Copper 1000 Mbit (Ethernet only) 4 = 10 GbE/SX 5 = 10 GbE/LR
	<b>E = FPGA Speed (AMC523)</b> 1 = Reserved 2 = High 3 = Highest***	
<b>C = Front Panel</b> 1 = Reserved 2 = Reserved 3 = Reserved 4 = Reserved 5 = Mid-size, MTCA.4 (captive screw) 6 = Full-size, MTCA.4 (captive screw)	<b>F = PCIe Fabric (AMC523)</b> 0 = No PCIe** 1 = PCIe on Ports 4-7 2 = PCIe on Ports 8-11 3 = PCIe on Ports 4-11	<b>J = Temperature Range and Coating (AMC523/MRT523)</b> 0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Reserved 7 = Reserved

Notes: \*Contact VadaTech sales for full range of mezzanine cards available

\*\*Only select when developing your own FPGA code

\*\*\*Minimum order quantity required

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

## Related Products

AMC725



- Double module, mid-size per AMC.0 and MTCA.4
- Intel® Xeon E3 processor options with PCH
- DVI graphics (SM750 w/16 MB DDR), up to 1920x1440 resolution

CM045



- Data Processing AMC in double module, mid-size (full-size optional)
- Compliant to MicroTCA.4
- Class D1.2 compatible

VT811



- MTCA System Platform 19" x 8U x 14.9" deep (with handles 16.23" deep)
- Full redundancy with dual MicroTCA Carrier Hub (MCH), dual Cooling Units and quad Power Modules
- Up to twelve AMCs: 12 front mid-size double module slots and RTM slots

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- Configurable solutions

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- Accelerated deployment
- AS9100 accredited



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DOC NO. 4FM737-12 REV 01 | VERSION 2.6 – AUG/19



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