

FMC217

FMC ADC 12-bit @ 6.4 GSPS and
DAC 16-bit @ 12 GSPS



FMC217

Key Features

- ADC ADC12DJ3200
 - Option for ADC12DJ2700
 - 8 JESD204B lanes from the ADC is routed to the FMC
 - 12-bit @ 6.4 GSPS
 - Wide full power bandwidth supports IF sampling of signals up to 6 GHz
- DAC AD9164/AD9162
 - 16-bit @ 12 GSPS
- FPGA Mezzanine Card (FMC) per VITA 57
- Excellent dynamic performance
- Front panel interface includes CLK In, Trig In and Trig Out

Benefits

- High dynamic range for versatility in video/broadcast requirements
- Ideal for Broadband communications systems, Wireless infrastructure, LTE, ATE, RADAR/Jamming
- Compatible with a broad range of Xilinx- and Altera-based FMC carriers from VadaTech and others
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company



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The FMC217 is an FMC per VITA 57 specification. The board has a dual channel ADC and single channel DAC.

The FMC217 utilizes TI ADC12DJ3200 ADC (with option for ADC12DJ2700) providing 12-bit conversion rates of up to 6.4 GSPS and a DAC AD9164 (option for AD9162) providing 16-bit conversion rates of up to 12 GSPS. The ADC in non-interleaving mode can have two separate inputs each at 3.2 GSPS.

The analog input/output, clock and trigger interfaces of the FMC217 are routed via SSMC connectors. The internal clock frequency is programmable and the clock is capable of locking to an external reference.

The module allows one of the inputs to be configured as Trigger Input or Output. Further the ADC TMSTP signal input source could be configured to come from the FPGA or the Trigger In.

The FMC217 has a front RF chain which include a programmable attenuator, RF amplifier, programmable attenuator followed by amplifier before it goes to the Balun. The RF chain is by passed with the F = 0 option. If the RF chain is on the front end of both ADC channels.



Figure 1: FMC217

Block Diagram

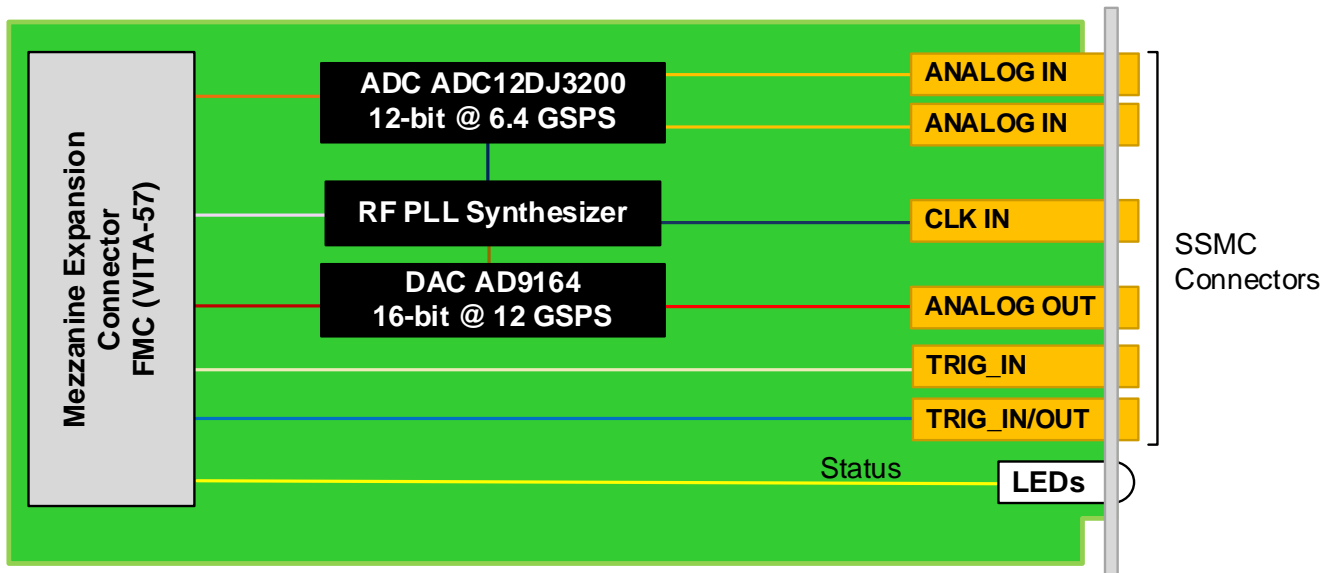


Figure 2: FMC217 Functional Block Diagram

Front Panel

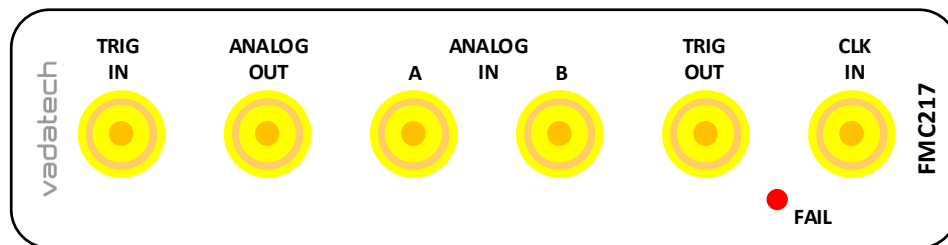


Figure 3: FMC217 Front Panel

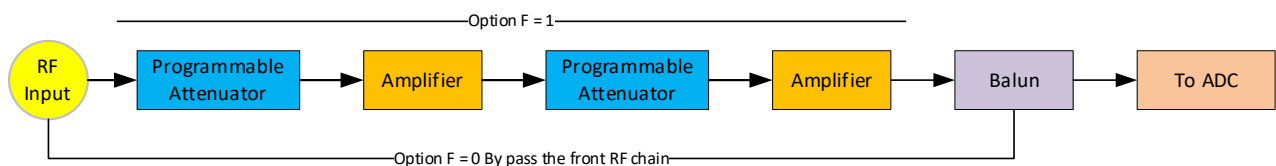


Figure 4: FMC217 Front end RF chain

Specifications

| | |
|-------------------------|---|
| Architecture | |
| Physical | Dimensions Single module Width: 2.71" (69 mm) Depth 3.01" (76.5 mm) |
| Type | FMC Dual-channel ADC with DAC, Single FMC |
| Standards | |
| FMC | VITA-57 ANSI/VITA 57.1-2008 |
| Configuration | |
| Power | FMC217 ~8W |
| Environmental | Temperature See ordering options (air flow requirements >400 LFM) and environmental spec sheet Storage Temperature: -40° to +85°C |
| | Vibration 1G, 5 to 500 Hz on each axis |
| | Shock 30Gs each axis |
| | Relative Humidity 5 to 95% non-condensing |
| Front Panel | Interface Connectors 6x SSMC |
| | LEDs Status |
| Software Support | Operating System Agnostic |
| Other | |
| MTBF | MIL Hand book 217-F@ TBD hrs |
| Certifications | Designed to meet FCC, CE and UL certifications, where applicable |
| Standards | VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards |
| Warranty | Two (2) years |

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

FMC217 – ABC-DE0-G0J

| A = TRIG*** | D = ADC Time Stamp source | G = FMC Board Spacing |
|--|---|--|
| 0 = Output 1 = Input | 0 = FPGA 1 = Trig In via front panel | 0 = 10 mm (per VITA 57 specification) 1 = 17.5 mm* |
| B = ADC | E = ADC Input | |
| 0 = ADC12DJ3200 (6.4 GSPS) 1 = ADC12DJ2700 (5.4 GSPS) 2 = Reserved | 0 = Standard ADC input 1 = Reserved | |
| C = DAC | F = Front RF | J = Temperature Range and Conformal Coating |
| 0 = AD9164 1 = AD9162 | 0 = Bypass front RF Chain 1 = Include the front RF Chain | 0 = Commercial (–5° to +55°C), No coating 1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70°C), No coating 4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane** 7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic** |

Notes: *For use with carriers that require higher mating clearance, such as VadaTech AMC595. Requires full size AMC.

**Conduction cooled, temperature is at edge of module. Consult factory for availability.

***One of the Triggers could be configured as input or output.

Related Products

AMC592



- AMC FPGA carrier for FMC per VITA 57
- Xilinx UltraScale™ XCKU115 FPGA
- Supported by DAQ Series™ data acquisition software

FMC214



- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) compatible

VPX592



- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

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DOC NO. 4FM737-12 REV 01 | VERSION 1.6 – MAY/23