

# VPX004

## 3U OpenVPX Switch, PCIe Gen 3 with Integrated Health Management



VPX004

## Key Features

- Unified 1 GHz quad-core CPU for, Shelf Manager, and Fabric management
- Automatic fail-over with redundant VPX004
- 1GbE base switch with dual 100/1000/10G uplink
- Full Layer 3 managed Ethernet switch
- Non-blocking PCIe Gen 3
- PLL synthesizer for generating any clock frequency disciplined to GPS/SyncE/IEEE1588
- VITA 46 and VITA 65 compliant

## Benefits

- Sophisticated clocking features enabling GPS/IEEE1588/SyncE/NTP Grand Master Clock
- Optional Virtual JTAG capability for remote programming and debugging eases FPGA code development
- VadaTech's Scorpionware® Shelf Management Software included at no additional cost
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company



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# VPX004

The VadaTech VPX00x family, with integrated health management, are the most feature-rich VPX Switch products on the market. The management software is based on VadaTech's robust Carrier Manager and Shelf Manager which have been deployed for years with proven results.

The MCMC manages the Power Modules, Cooling Units, and up to 12 payload modules within the chassis. It also manages the PCIe Gen3 switch and the standard GbE with 10GbE uplink Base Channel switch.

The Ethernet switch is managed with an enterprise grade Layer 2 or 3 switching/routing stack which supports Synchronous Ethernet.

The unit runs Linux on its centralized quad-core CPU and is fully redundant when used in conjunction with a second instance of the module. The firmware is HPM.2 compliant that allows for easy upgrades.

VPX004 provides optional Master JTAG services to the payload modules via the JSM and has advanced clocking features including grand master clock and high-quality clock distribution/synthesis.



Figure 1: VPX004

# Block Diagram

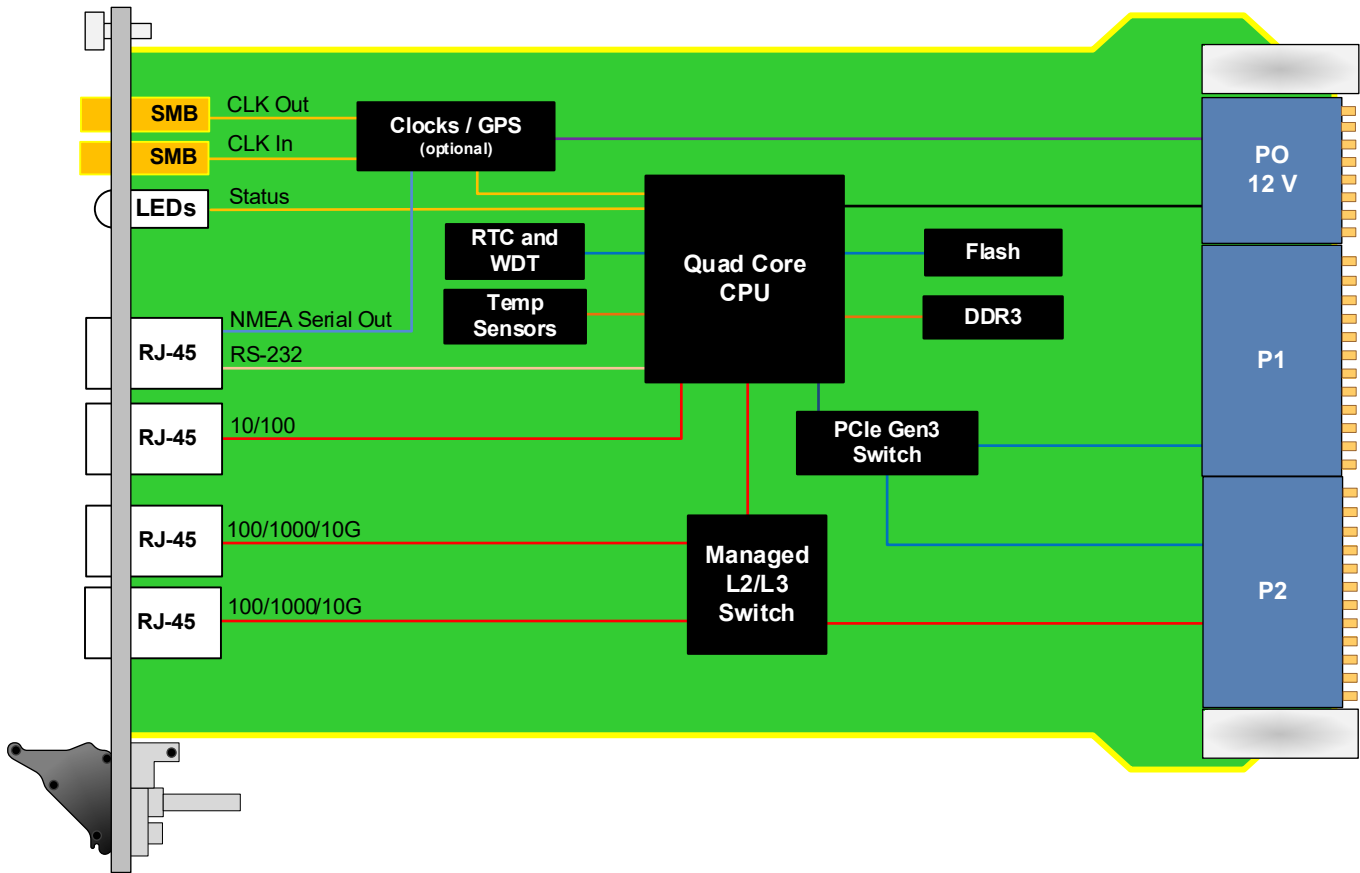


Figure 2: VPX004 Functional Block Diagram

# Front Panel

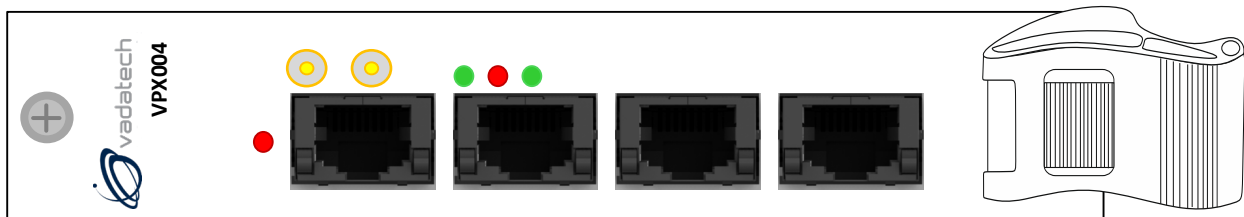


Figure 3: VPX004 Front Panel

# Architecture

## IPMI Carrier Manager, Shelf Manager and Protocol Analyzer

The VPX004 utilizes the same proven standards-compliant IPMI management stack that has been utilized successfully in our previous generation products. It supports carrier manager, shelf manager, and protocol analyzer operations to help facilitate a seamless chassis integration experience. The IPMI stack enables a rich feature set including:

- IPMI v2.0 with IPMI v1.5 compatibility
- SDR, FRU, and SEL storage interfaces (SEL stored in MRAM for high-speed/non-volatile/no-wear-out access)
- Intelligent temperature, voltage, and current sensing
- Shelf cooling policy
- Shelf activation and power management/Automatic fail-over/redundancy management
- Alarm controls
- Event notification and flexible alerting policies
- CLI, SNMP, RMCP+, HTTP, and HPI
- IPMB Protocol Analyzer GUI for use on PC
- ScorpionWare GUI system manager integration tool on PC available separately

## Base Channel Ethernet Switch

The VPX004 provides as standard a GbE base channel switch. This switch is fully Layer 3 managed enabling a comprehensive enterprise-grade routing and switching feature set. It supports Synchronous Ethernet (SyncE) and IEEE1588.

## Fat Pipe Fabric

The VPX004 PCIe Gen3 Switch provides:

- Speed setting for 2.5/5/8 Gbps per lane
- Virtual Switch/Multiple domain/Non-transparent port support to enable partitioning of the system with multiple root complexes
- Includes an extra internal port which enables the GPS precision time-stamping engine (accessible from an VPX root complex board)
- 192 Gbps aggregate bandwidth/non-blocking/cut-through architecture

## Fabric Clock Option

The VPX004 has the capability to provide a 100 MHz HCSL PCIe Gen3-compliant fabric clock to each VPX. This option enables the recommended synchronous PCIe clocking approach within the chassis when used in combination with the PCIe fabric.

## GPS and General-Purpose Clocks

The VadaTech VPX004 has the most sophisticated clocking distribution in the market to meet the most stringent requirements such as wireless infrastructure, high speed A/D, etc. The VPX004 supports the following GPS and general-purpose clocking features:

- Open VPX-compliant low-jitter/low-skew backplane routing
- Clock disciplining with arbitrary clock frequency output and holdover (Stratum-3 option) including 1PPS regeneration and holdover
- Flexible integration and synchronization between GPS, IEEE1588/SyncE, and NTP clocking enabling Grand Master clock functionality
- 'Any Frequency' high-quality clock generation/jitter cleaning for up to two user clocks
- Supports hitless automatic clock failover for improved reliability
- Optional built-in GPS receiver enables direct time/clock synchronization to the GPS satellite constellation

The VPX004 supports flexible front panel clock port ordering options:

- Two DC-coupled LVCMOS Inputs/Outputs, or two AC-coupled Sine-wave Inputs, or one of each
- Built-in GPS receiver for time/location/clock synchronization plus a DC-coupled LVCMOS Input/Output

## GPS Receiver Enabled Features

The VPX004 can be ordered with a GPS Receiver option. The receiver disciplines an onboard high-quality DPLL which is phase/frequency aligned to the atomic clocks in the GPS satellite constellation. The onboard clock synthesis/jitter cleaning capability can be utilized to convert this frequency into any frequency desired while still remaining locked to the GPS atomic clocks.

When the GPS Receiver option is purchased the VPX004 has the capability to re-transmit the incoming GPS data via Ethernet to other network nodes in the Trimble TSIP binary protocol format. This GPS data is also sent out the front panel GPS RS-232 serial port in the standard NMEA format for use by external equipment. When the GPS Receiver option is purchased along with the PCIe fabric, the VPX Switch also provides a precision PCIe Timestamping Engine capability to a PCIe Root Complex on the backplane. This engine appears as a PCIe device to the VPX card and a device driver is available which will allow the VPX card to read all GPS status including position, velocity, status, etc., in addition to precision timestamps, time trigger, and time event interrupt functionalities.

## IEEE1588 PTP and NTP Grand Master Clock

The VPX004 provides Ethernet time service to the chassis network on the GbE fabric port. It can be subordinate to an external PTP or NTP master server or when the GPS receiver option is purchased can act as a Grand Master clock utilizing the precision timing information provided via the GPS receiver and onboard disciplined oscillator.

## Synchronous Ethernet

The VPX004 provides a Synchronous Ethernet (SyncE) on the GbE fabric port. With this feature, ports on the 1G Ethernet switch can be designated as master or slave ports and the Ethernet fabrics within the chassis can be synchronized from end-to-end with external equipment. This feature utilizes advanced telecom-grade network synchronization PLLs to provide exceptional SyncE performance.

## JTAG Master/JTAG via Ethernet Virtual Probe

The VPX004 provide JTAG Master Capability to send out configuration data streams via the chassis JTAG Switch Module (JSM) to configure arbitrary JTAG Slave devices on VPX cards. Virtual Probe services are also optionally available to provide JTAG via Ethernet for Xilinx FPGAs. This allows for standard development tools such as Xilinx iMPACT/ChipScope to treat the switch/JSM combination as if it was a standard JTAG probe. This approach frees the developer from having to attach JTAG probes directly to the VPX module or JSM which can be difficult when systems are already fully assembled. It also allows for remote debugging across long distances when required without the need to install additional JTAG equipment on-site.

# Specifications

Architecture		
<b>Physical</b>	<b>Dimensions</b>	3U, 1" pitch
<b>Type</b>	<b>Controller</b>	OpenVPX Switch with Integrated Health Management
Standards		
<b>VPX</b>	<b>Type</b>	VITA 46.x
<b>VPX</b>	<b>Type</b>	VITA 65 OpenVPX
<b>Module Management</b>	<b>IPMI</b>	IPMI v2.0 HPM v1.0
Configuration		
<b>Power</b>		Option load dependent (as the MCMC and GBE <20W) On P0; VS1 = 12V
<b>Front Panel</b>	<b>Interface Connectors</b>	Option Clocks/GPS NMEA serial data out (RJ-45) Two CLK IN/OUT (SMB); CLK IN becomes GPS ANT IN with GPS receiver option LEDs Status CPU RS-232 (RJ-45) 100/1000/10G x2 from L2/L3 Base Switch Fabric (RJ-45) and CPU 10/100 (RJ-45)
<b>VPX Interfaces</b>	<b>Slot Profiles</b>	See <a href="#">Ordering Options</a>
	<b>Rear IO</b>	IPMI on P0; JTAG on P0 Clocks/GPS (Optional) on P0 PCIe Gen 3 on P1/P2 Managed L2/L3 Switch on P2
<b>Software Support</b>	<b>Operating System</b>	Linux
Other		
<b>MTBF</b>		MIL Hand book 217-F@ TBD hrs
<b>Certifications</b>		Designed to meet FCC, CE and UL certifications, where applicable
<b>Standards</b>		VadaTech is certified to both the ISO9001:2015 and AS9100D standards
<b>Warranty</b>		Two (2) years, see <a href="#">VadaTech Terms and Conditions</a>

## INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

# Ordering Options

## VPX004 – ABC-DEF-GHJ

<b>A = Fabric Switch (Fat Pipes)</b> 0 = No fabric switch 1 = PCIe Gen 3	<b>D = Front Panel Clocking</b> 0 = No Clocking 1 = Dual LVCMOS Clock In/Out 2 = Sine Wave In + LVCMOS In/Out 3 = Built-in GPS receiver + LVCMOS In/Out 4 = Dual Sine Wave In 5 = GPS receiver + Sine Wave In 6 = Sine Wave In (up to 17dBm) +TTL/LVCMOS In	<b>G = Applicable Slot Profile</b> 0 = 5HP, IEEE 1101.10 1 = 5HP, VITA 48.1
<b>B = GbE Switch (Thin Pipes)</b> 0 = GbE Included 1 = No GbE	<b>E = Clock Holdover Stability</b> 0 = Standard (XO) 1 = Stratum-3 (TCXO)	<b>H = Environmental</b> See <a href="#">Environmental Specification</a>
<b>C = VPX Connector Type</b> 0 = Standard 50u Gold Rugged 1 = KVPX Connectors	<b>F = JTAG Virtual Probe</b> 0 = No JTAG Virtual Probe 1 = JTAG Virtual Probe Included	<b>J = Conformal Coating</b> 0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

## Environmental Specification

Option H	Air Cooled			Conduction Cooled	
	H = 0	H = 1	H = 2	H = 3	H = 4
<b>Operating Temperature</b>	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
<b>Storage Temperature</b>	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
<b>Operating Vibration</b>	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
<b>Storage Vibration</b>	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
<b>Humidity</b>	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

**Notes:**

\*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

## Related Products

VPX516



- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX518



- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Zynq-7000 FPGA in FFG-900 package (XC7Z100 or XC7Z045)
- High-performance clock jitter cleaner

VPX599



- 3U FPGA Dual DAC and dual ADC per VITA 46
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS



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