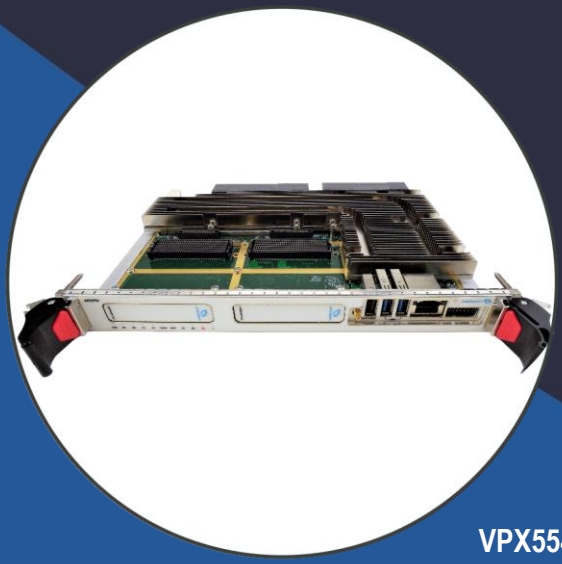
# VPX554

## Xilinx Virtex UltraScale+™ XCVU47P, CPU NXP LX2160A with Dual FMC+, 6U VPX



VPX554

## Key Features

- Xilinx Virtex UltraScale+™ XCVU47P FPGA with 16GB of High Bandwidth Memory (HBM)
- Processor Layerscape LX2160A (16-core, ARM Cortex A72 Core) @ 2.2GHz per core
- Dual FMC+ per VITA 57.4
- From FPGA dual 100G/40G/10G speed to the rear via VITA66.5 optical (P6 Location)
- CPU with 32GB of DDR4 with ECC
- 8GB of eMMC
- 1TB of NVMe
- Dual USB 3.0/2.0 with dual RS-422/485 (to P2)
- 12x RX/TX SERDES from FPGA to P3
- Additional 16GB of DDR-4 to FPGA
- Differential and/or single I/O to P4/P5
- Clock PLL jitter cleaner
- Health Management through dedicated processor

## Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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# VPX554

The VPX554 is a 6U VPX board utilizing Xilinx Virtex UltraScale+™ XCVU47P FPGA with CPU from NXP LX2160A.

The VPX554 has dual FMC+ sites per VITA57.4 which route all the LA/HA/HB as well as all the FMC+ 32 SERDES (DP) to the FPGA.

The FPGA XCVU47P has integrated 16GB of High Bandwidth Memory (HBM) which can provide large memory buffer space. In addition, the FPGA has 16GB of DDR4 memory. The FPGA has 12x SERDES routed to the P6 location via VITA 66.5 optical. These SERDES could utilize the hardcore CMAC of the XCVU47P to run at 100GbE or as 40GbE/10GbE, Aurora, etc. The FPGA has 12 additional RX/TX SERDES routed to P3 which could operate up to 28Gbaud per lane. Ports 0-3 of the P3 connector are routed to the FPGA PCIe Hardcore. The FPGA routes to P4/P5 16x LVDS (which could be configured as single ended lanes vs. differential per pair) as well as additional singled ended 48x GPIO which could be configured in banks of x8 as +3.3V or +5V.

The CPU is based on the NXP LX2160A which has 16 A72 cores running at 2.2GHz each.

The health management CPU, the LX2160A CPU and the FPGA RS-232 are routed to a USB-to-RS-232 interface which is accessed through USB 2.0.

The VPX554 has a PLL clock jitter cleaner and can provide clocks to both of the FMCs, the FPGA, and/or the protocol clocks for P0/P4 connectors.

The health management is based on the VITA 46.11 with Tier 2 support.

The unit is available in a range of temperature and shock/vibe specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

*Figure 1: VPX554*


*Figure 2: VPX554 Front Panel View*

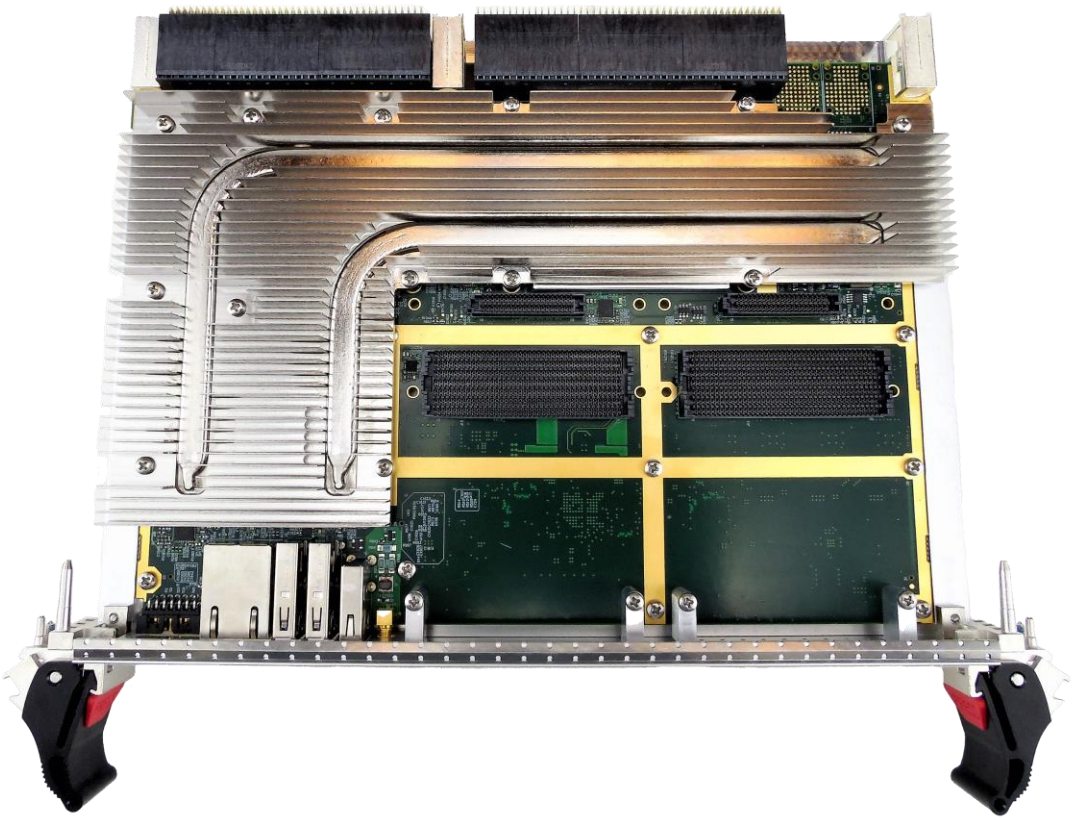

*Figure 3: VPX554 Top View with Heatsink*


*Figure 4: VPX554 Top View without Heatsink*

# Block Diagram

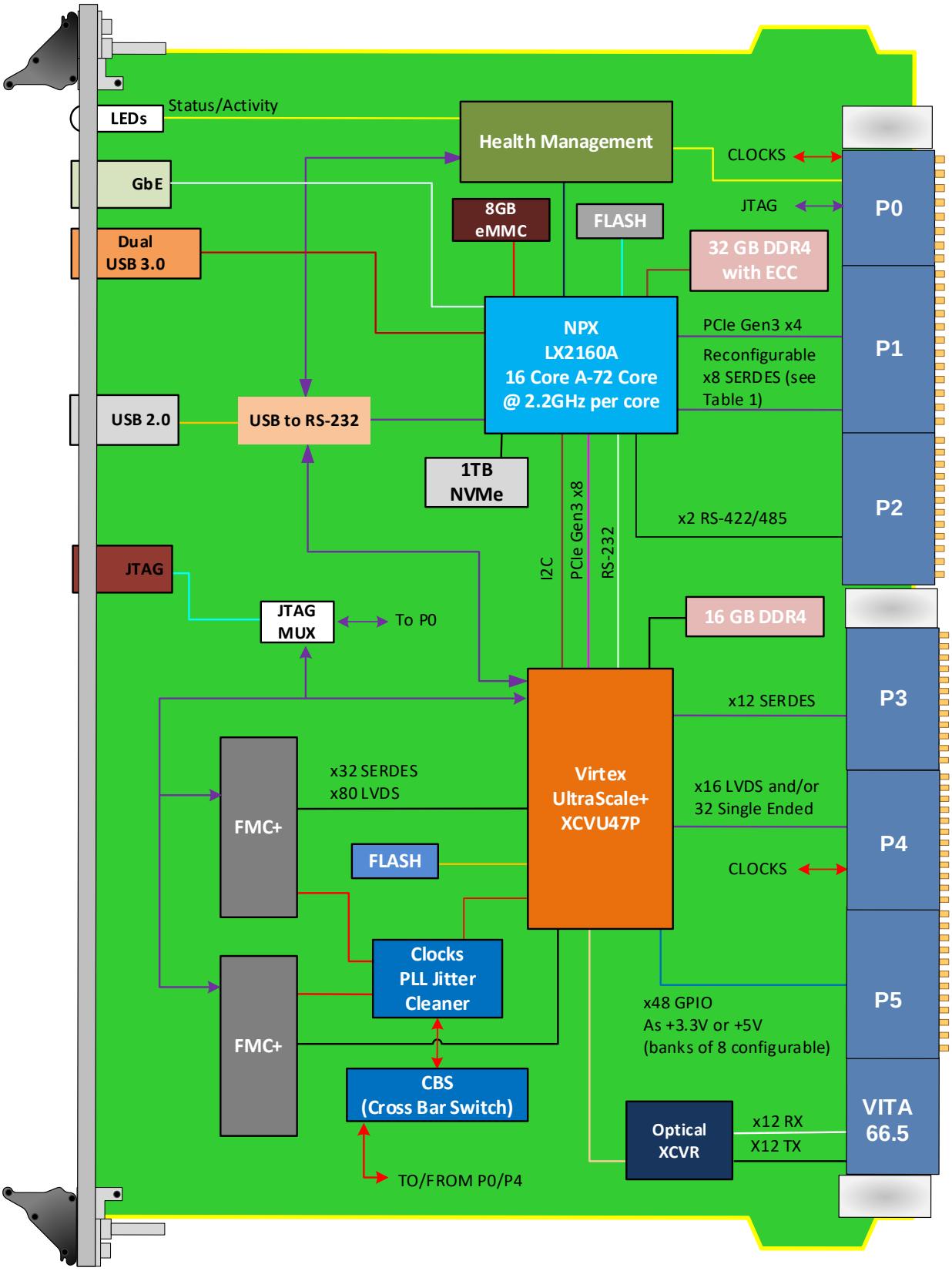


*Figure 5: VPX554 Functional Block Diagram*

| Option F = | Configuration for the 8x reconfigurable SERDES (CPU) |
|---|---|
| 0 | Dual PCIe Gen3 x4 |
| 1 | 4x GbE with PCIe Gen3 x4 |
| 2 | 4x 10GBASE-KR with PCIe Gen3 x4 |
| 3 | 8x GbE |
| 4 | PCIe Gen3 x4 with 4x 10GBASE-KR |
| 5 | 4x 10GBASE-KR with 4x GbE |
| 6 | 8x 10GBASE-KR |
| 7 | PCIe Gen3 x4 with PCIe Gen2 x2 with 2x GbE |
| 8 | 2x 40GBASE-KR4 |
| 9 | Reserved (other options are possible, please contact VadaTech Sales) |

*Table 1: Ordering Option F for reconfigurable x8 SERDES (CPU)*

# Reference Design

VadaTech provides an extensive range of Xilinx-based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high-speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and OpenVPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

# Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

# Specifications

| | | |
|---|---|---|
| **Architecture** | | |
| **Physical** | **Dimensions** | 6U, VPX |
| **FPGA** | | Xilinx Virtex UltraScale+™ XCVU47P |
| **Configuration** | | |
| **Power** | **VPX554** | ~85W (CPU and FPGA load dependent) |
| **Front Panel** | **JTAG** | Standard JTAG header via front or P0 |
| | **USB 2.0** | RS-232 from Health Management; CPU; FPGA |
| | **USB 3.0** | Dual USB 3.0 |
| | **GbE** | RJ-45 |
| | **FMC+0** | FMC+ front I/O site 0 |
| | **FMC+1** | FMC+ front I/O site 1 |
| | **LEDs** | User defined by the FPGA and Health Management |
| **VPX Interfaces** | **Slot Profiles** | See Ordering Options |
| | **Rear IO** | P1: x4 PCIe Gen3 and x8 Reconfigurable SERDES |
| | | P2: x2 RS422/485 |
| | | P3: x12 SERDES (up to 28Gbaud per lane) |
| | | P4: x16 LVDS and/or 32 single ended (+1.8V) |
| | | P5: x48 Single ended configurable as +3.3V or +5V per x8 configuration |
| | | P6 : VITA66.5 12RX/TX |
| **Software Support** | **Operating System** | Linux (default) or VxWorks |
| **Other** | | |
| **MTBF** | MIL Hand book 217-F@ TBD hrs | |
| **Certifications** | Designed to meet FCC, CE and UL certifications, where applicable | |
| **Standards** | VadaTech is certified to both the ISO9001:2015 and AS9100D standards | |
| **Warranty** | Two (2) years, see VadaTech Terms and Conditions | |

OpenVPX allows for a wide range of pin assignments and use cases. Prior to purchasing VadaTech products as standalone items (i.e. not part of an integrated platform) please consult with VadaTech on the system architecture to ensure compatibility.

### INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

# Ordering Options

## VPX554 – ABC-DEF-GHJ

| A = Processor | D = FPGA Speed | G = Applicable Slot Profiles |
|---|---|---|
| 0 = Reserved<br>1 = LX2160A, 2.2GHz with Security Engine | 1 = Reserved<br>2 = High<br>3 =Reserved | 0 = 5 HP, VITA 48.1 |
| **B = P3 Connector FPGA SERDES Configuration** | **E = VITA 66.5 Optical Modules** | **H = Environmental** |
| 0 = No PCIe<br>1 = x4 PCIe port 0-3 (FPGA Hard Core) | 0 = Not installed<br>1 = x12 TX/RX | See Environmental Specification |
| **C = VPX Connector Type** | **F = P1 Ports 8-15 Configuration** | **J = Conformal Coating** |
| 0 = Standard 50u Gold Rugged**<br>1 = KVPX Connectors | Per Table 1 | 0 = No coating<br>1 = Humiseal 1A33 Polyurethane<br>2 = Humiseal 1B31 Acrylic |

**Notes:**

For operational reasons VadaTech reserves the right to supply a higher speed FPGA device than specified on any particular order/delivery at no additional cost, unless the customer has entered into a Revision Lock agreement with respect to this product.

**P3 has the high speed (25G) connectors

## Environmental Specification

| | Air Cooled | | Conduction Cooled | | |
|---|---|---|---|---|---|
| **Option H** | **H = 0** | **H = 1** | **H = 2** | **H = 3** | **H = 4** |
| **Operating Temperature** | AC1* (0°C to +55°C) | AC3* (-40°C to +70°C) | CC1* (0°C to +55°C) | CC3* (-40°C to +70°C) | CC4* (-40°C to +85°C) |
| **Storage Temperature** | C1* (-40°C to +85°C) | C3* (-50°C to +100°C) | C1* (-40°C to +85°C) | C3* (-50°C to +100°C) | C3* (-50°C to +100°C) |
| **Operating Vibration** | V2* (0.04 g2/Hz max) | V2* (0.04 g2/Hz max) | V3* (0.1 g2/Hz max) | V3* (0.1 g2/Hz max) | V3 (0.1 g2/Hz max) |
| **Storage Vibration** | OS1* (20g) | OS1* (20g) | OS2* (40g) | OS2* (40g) | OS2* (40g) |
| **Humidity** | 95% non-condensing | 95% non-condensing | 95% non-condensing | 95% non-condensing | 95% non-condensing |

**Notes:**

*Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

# Related Products

VPX551

- Dual Kintex UltraScale™ XCKU115
- 16 GB of 64-bit wide DDR4 Memory to each FPGA
- Rear fibre I/O via VITA 66.5

VPX980

- Quad Core ARM Freescale processor @ 1 GHz per core
- One GB DDR3 memory with FRAM for log messages
- 32 GB of Flash, 8 GB of NAND Flash

VTX990

- One slot benchtop 6U VPX development platform
- P0 to P6 connectors are installed
- Variable fan speed control for front and rear

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