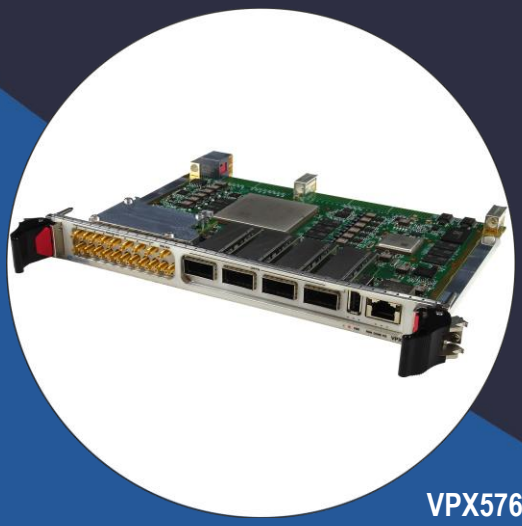
VPX576

Virtex UltraScale+ FPGA with Octal ADC/DAC in 6U VPX



VPX576

Key Features

- Xilinx XCVU13P UltraScale+
- Two banks of DDR4 Memory 16GB total
  - Single Bank of 64-bit wide 8GB
  - Single Bank of 32-bit wide 4GB
- Four QSFP28 (4x 100GbE)
- Dual Analog Device AD9081
  - 8 ADC/DAC fully synchronized
  - Direct RF CLK
- Xilinx Zynq UltraScale+ XCZU04CG
- 8GB of DDR4 with ECC
- 64GB of SSD
- Health Management through dedicated Processor

Benefits

- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX576

The VPX576 is a 6U VPX FPGA based on Xilinx XCVU13P FPGA with front I/O access. The module has an on-board, reconfigurable FPGA which interfaces directly to the VPX P1/P2/P3/P4 with high speed SERDES and LVDS/Single ended to P5. The SERDES are configurable to run multiple protocols such as PCIe, Aurora, SRIO, XAUI, 40G, 100G, etc. For the PCIe option the module could run as single x16/x8/x4.

The FPGA interfaces with two Analog Device AD9081 devices. The module takes direct RF Clock and distributes across the two devices. The two devices are synchronized.

The FPGA has dual bank of DDR-4 with total of 12GB. A single bank of DDR-4 64-bit wide (8GB) and single bank of DDR-4 32-bit wide (4GB).

The DACs could run @ 12 GSPS 16-bit wide and the ADCs could run @ 4 GSPS 12-bit wide.

The VPX576 has Quad QSFP28 ports in the front which could run as 100Gb Ethernet or any other protocols such as Aurora, SRIO, etc.

Further the module has a Zynq UltraScale+ FPGA which interfaces to the VU13 via x1 PCIe, dual x2 SERDES as well as single ended. The ZU04 has two GbE which is routed from the PS side to the P1 ports 15/16 and dual SERDES to the P1 Ports 13/14 from the PL side.

Onboard microcontroller implements Tier-2 health management.

Figure 1: VPX576

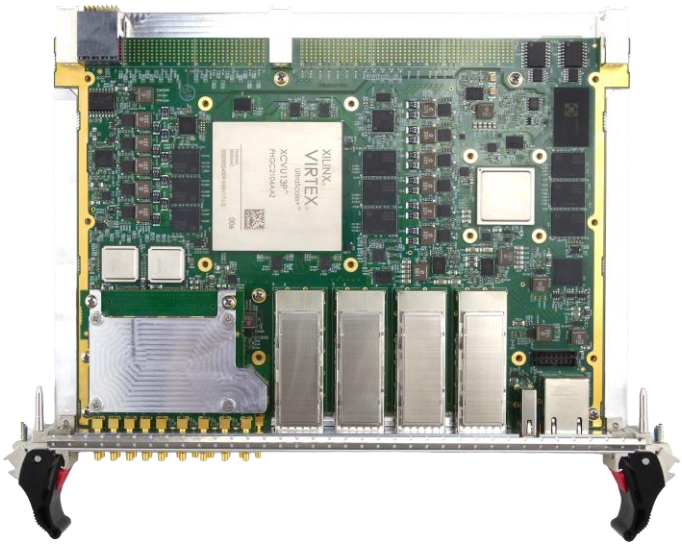


Figure 2: VPX576 Top View

Block Diagram

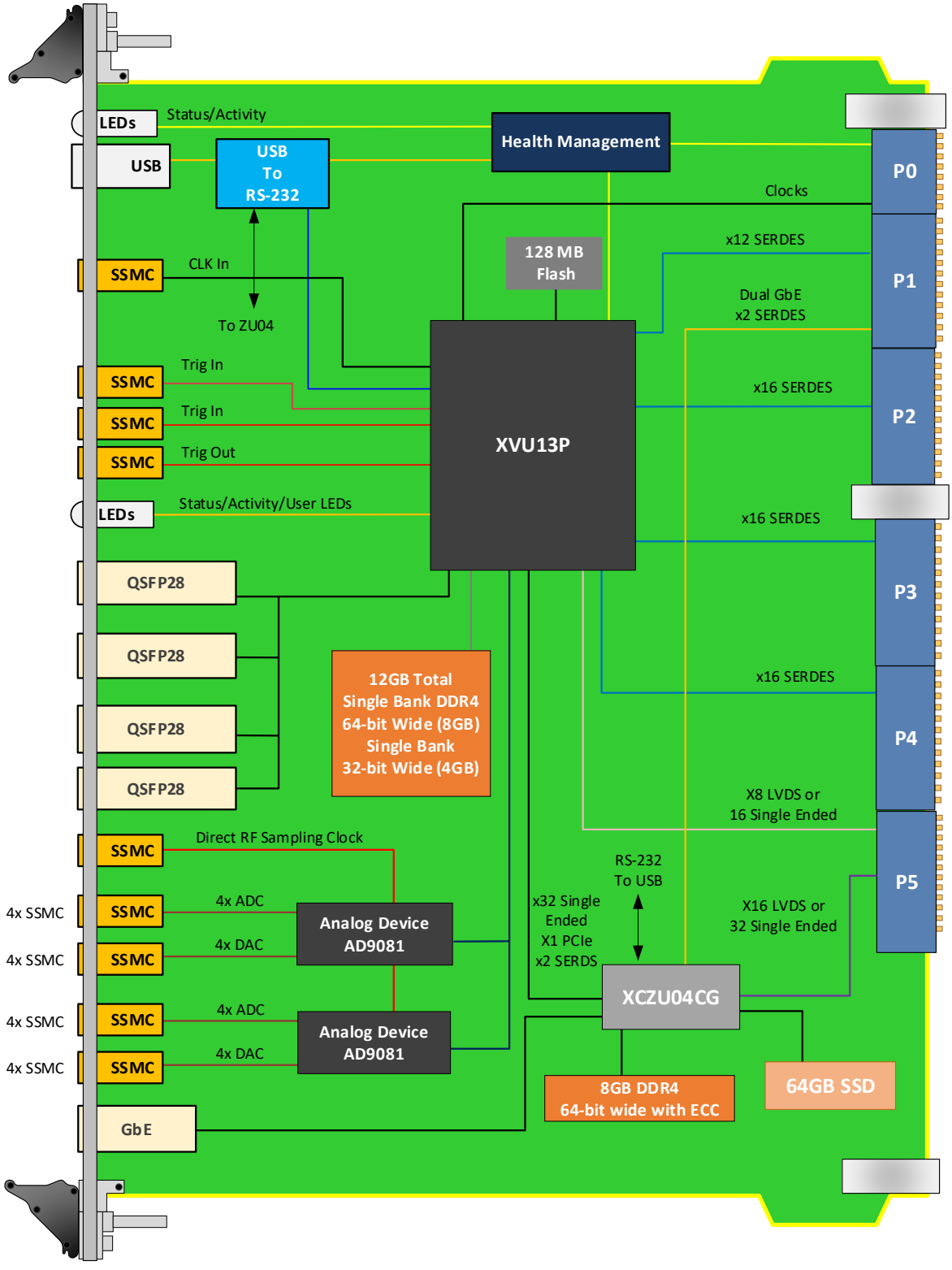
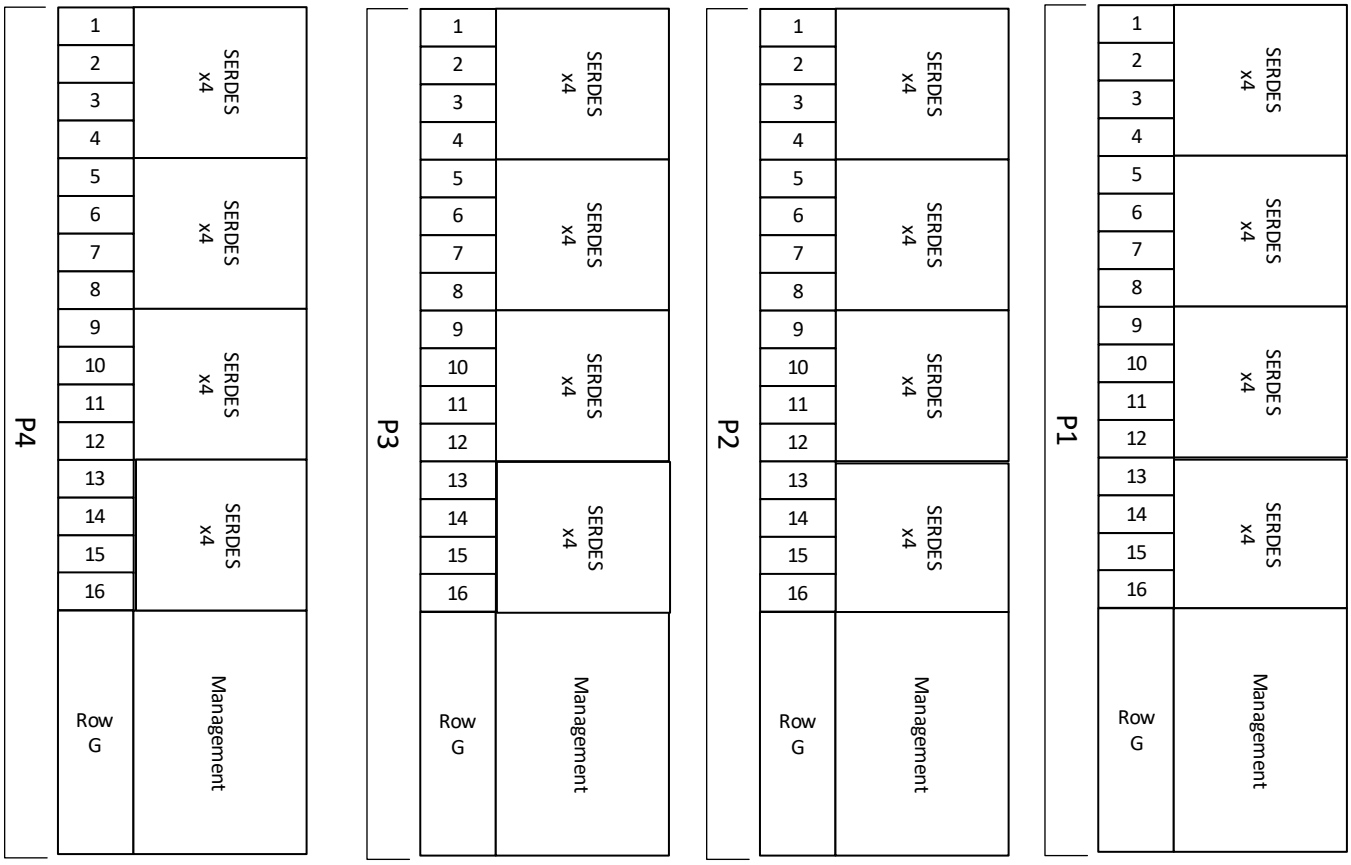


Figure 3: VPX576 Functional Block Diagram

Pinout Block Diagram



Front Panel

Figure 4: VPX576 Front Panel View

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	6U, 1” pitch
Type	**FPGA**	Xilinx Virtex UltraScale+ XCVU13P
Configuration		
Power	**VPX576**	90W FPGA load dependent
Front Panel	**Interface Connectors**	Quad QSFP28
		2x RS-232
		16x SSMC for ADC/DAC
		4x SSMC for Trig In/Out and CLK input
	LEDs	User defined by the FPGA and Health Management
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P0: IPMB for Health Management and CLK
		P1/2/3/4: High speed SERDES
		P5: LVDS and/or Single ended
Software Support	**Operating System**	Agnostic
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX576 – ABC-DEF-GHJ-KLM-N00

A = P1/P2 Connectors	D = FPGA Speed	G = PCIe ZU04 Ports 13/14 to P1	K = QSFP28 Transceivers***
0 = P1/P2 Not loaded 1 = P1/P2 Loaded 2 = P1 Loaded 3 = P2 Loaded	1 = Reserved 2 = High (-2L) 3 = High (-2) 4 = Highest (-3)*	0 = No PCIe 1 = PCIe	0 = None 1 = 100G SR 2 = 100G LR (1km) 3 = 100G WDM (SR) 4 = Reserved
B = P3/P4/P5 Connectors*	**E = PCIe Option P1/P2**	**H = Environmental**	**L = DAC Portion**
0 = P3/P4/P5 Not loaded 1 = P3/P4/P5 loaded 2 = P5 loaded 3 = Reserved	0 = No PCIe 1 = PCIe 1-4 ports (PCIe x4) 2 = PCIe 1-8 ports (PCIe x8) 3 = PCIe 1-16 ports (PCIe x16) P2 Only	See Environmental Specification	0 = Not used 1 = DAC is utilized
C = Front End Balun	**F = PCIe Option P4**	**J = Conformal Coating**	**M = RF Clock input range**
0 = 500KHz to 9GHz Marki 1:1 ratio 1 = 500KHz to 9GHz Marki 1:2 ratio 2 = 500KHz to 6GHz Marki 1:1 ratio 3 = 500KHz to 6GHz Marki 1:2 ratio 4 = 500KHz to 3GHz Marki 1:1 ratio 5 = 500KHz to 3GHz Marki 1:2 ratio 6= Reserved	0 = No PCIe 1 = PCIe 1-4 ports (PCIe x4) 2 = PCIe 1-8 ports (PCIe x8)	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic	0 = 2GHz to 6.5GHz 1 = 6.6GHz to 12GHz
N = Pitch			
0 = 5 HP (1" standard) 1 = 10 HP (2" double size)			

* Minimum order qty needed
** For other option please contact VadaTech Sales
***Four Transceivers are included. For other options please contact VadaTech Sales

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

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