VPX597

300 MHz to 6 GHz Octal Versatile Wideband Transceiver (MIMO), Kintex UltraScale™, 3U VPX

VPX597

Key Features

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Four AD9371s or AD9375s on one module
- Octo complete transceiver signal chain solution
- Tx synthesis bandwidth to 250 MHz
- Rx bandwidth: 8 MHz to 100 MHz
- Health Management through dedicated Processor

Benefits

- High density transceiver with intensive data processing capability
- Observation channels for implementation of error correction functions
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

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VPX597

The VPX597 is a wideband transceiver in 3U VPX form factor. The unit contains four AD9371s connected to a Kintex UltraScale™ XCKU115 FPGA providing eight transceiver channels. This makes the unit suitable for applications such as SDR, BTS, antenna systems, research and instrumentation.

The re-configurable FPGA has direct interface with the wideband transceivers (via JESD204B) along with two banks of DDR4 memory. This allows for large buffer sizes to be stored during processing as well as queuing the data to the host connectors.

VPX597 routes x16 high speed SERDES to P1 that can be configured as PCIe/SRIO/10GbE/Aurora, etc. The module routes an additional x8 SERDES, x16 GPIO and x8 LVDS to P2. The dedicated onboard health management CPU is OpenVPX standard compliant.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

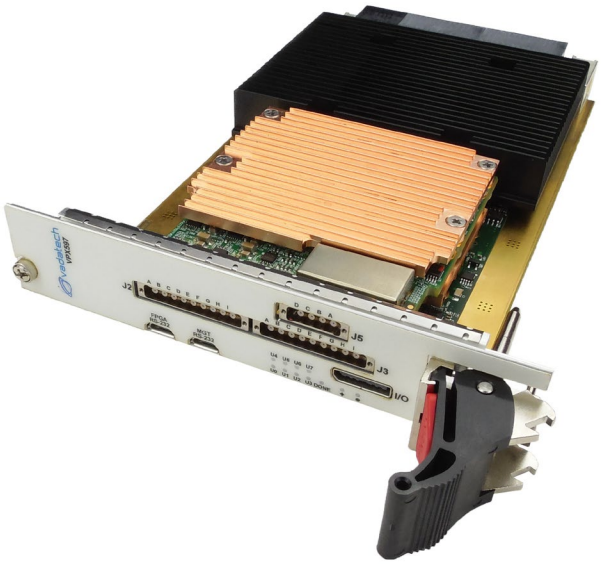

Figure 1: VPX597

Block Diagram

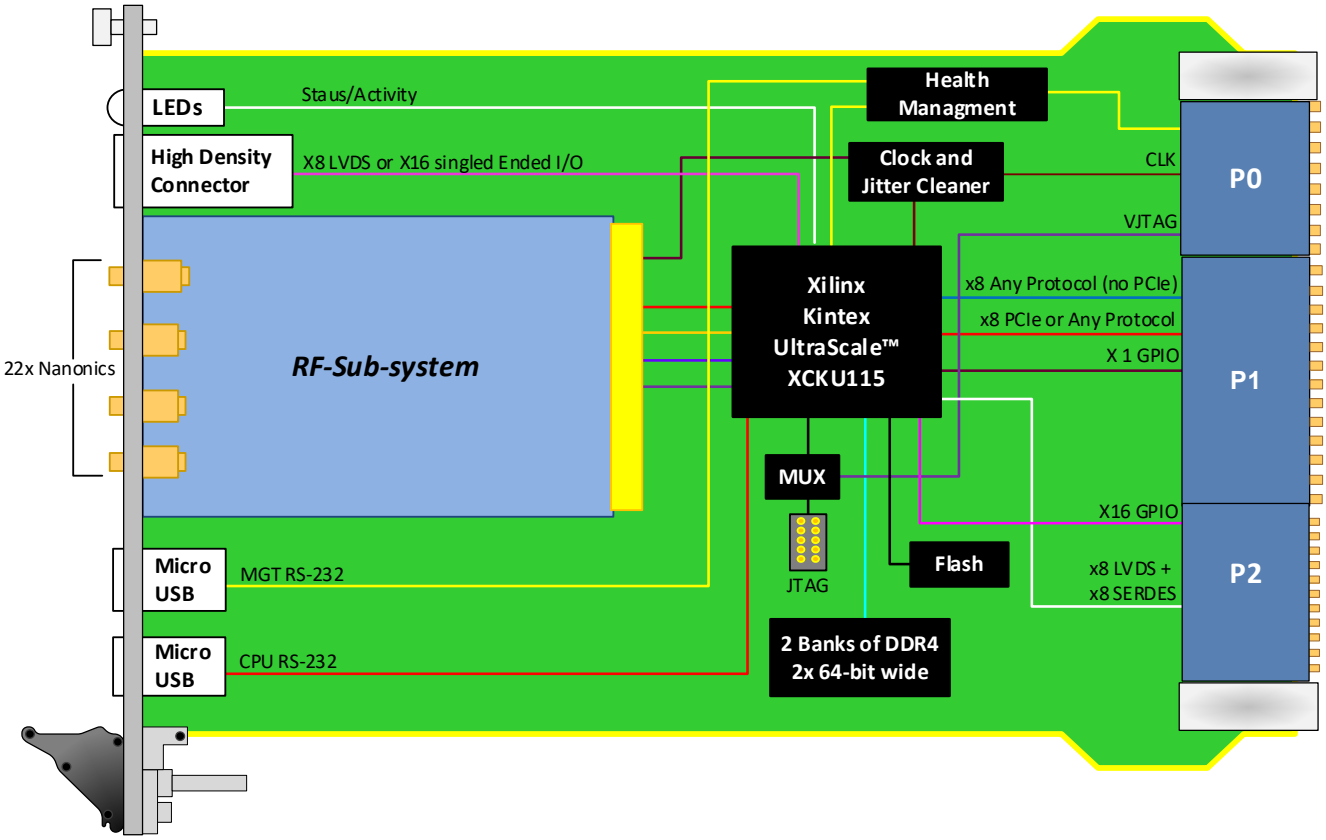

Figure 2: VPX597 Functional Block Diagram

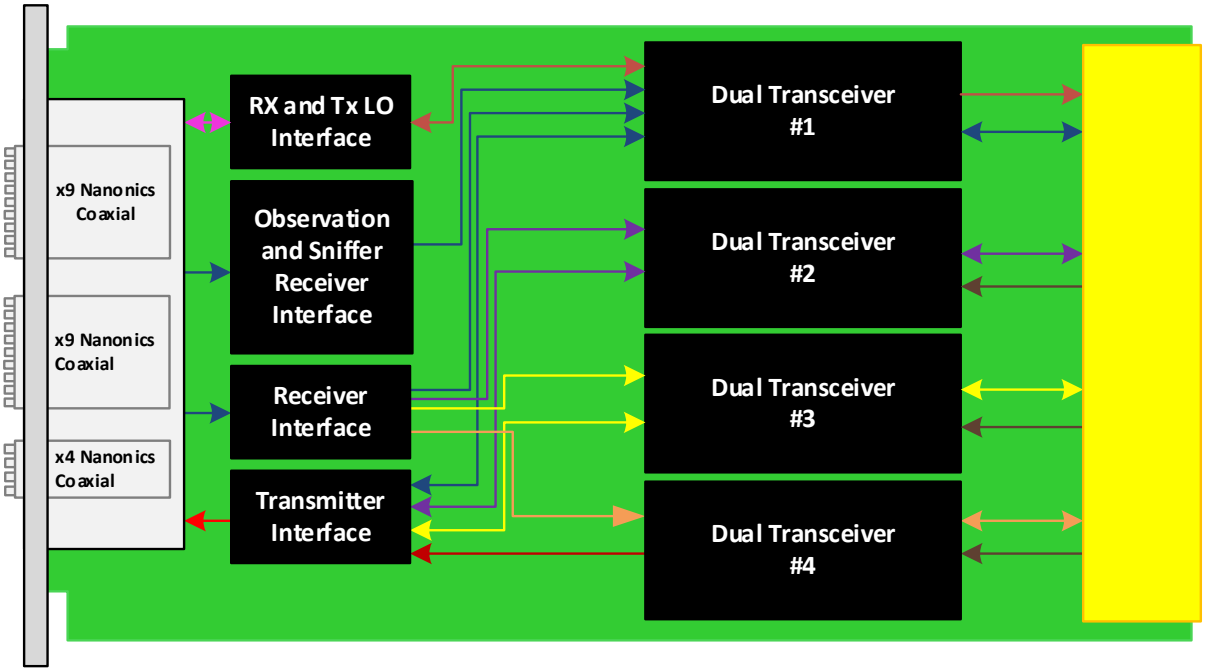

Figure 3: VPX597 RF Sub-system Block Diagram

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can be accessed from the customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

The VPX597 is compatible with Analog Devices design tools for AD9371.

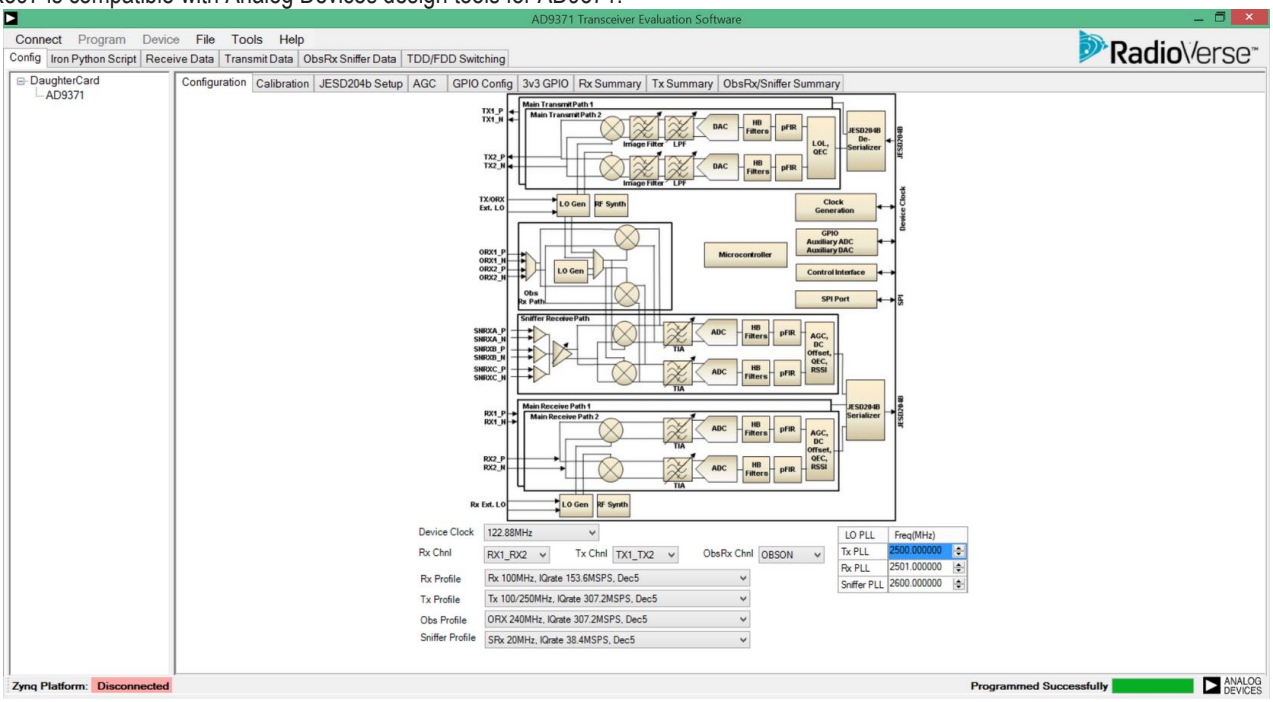

Figure 4: Compatible Analog Devices for AD9371

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
FPGA		Xilinx Kintex UltraScale™ XCKU115
Configuration		
Power		~40W (dependent on FPGA load), 65W maximum
Memory		Two banks of DDR4, 64-bit wide (16 GB total)
Front Panel		22 Nanonics Coaxial
	Micro USB	RS-232 from Health Management and RS-232 from FPGA
	LEDs	User defined by the FPGA and Health Management
Onboard Interfaces		JTAG
VPX Interfaces	**Slot Profiles**	See Ordering Options
	Rear IO	P1: x8 high speed serial links (PCIe, 10GbE/SRIO/Aurora per FPGA load)
		P1: x8 high speed serial links (10GbE/SRIO/Aurora per FPGA load)
		P2: x8 high speed serial links (10GbE/SRIO/Aurora per FPGA load)
	Power Supplies	P0: VS1 = 12V
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2015 and AS9100D standards	
Warranty	Two (2) years, see VadaTech Terms and Conditions	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX597 – ABC-DEF-GHJ

A = RF Direct Clock Sampling	D = FPGA Speed	G = Applicable Slot Profiles
0 = Front Panel 1 = Onboard Wideband PLL	1 = Reserved 2 = High 3 = Highest	0 = 5 HP, IEEE 1101
B = MIMO Device	**E = Clock Holdover Stability**	**H = Environmental**
0 = AD9371 1 =AD9375	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification
C = VPX Connector Type	**F = PCIe Option (P1)***	**J = Conformal Coating**
0 = Standard 50u Gold Rugged 1 = KVPX Connectors	0 = No PCIe 1 = PCIe x4 2 = PCIe x8	0 = No coating 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Notes: *When the Ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC 12-bit @ 6.4 GSPS
- Dual DAC 16-bit @ 12 GSPS (AD9162 or AD9164)

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