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Solution Brief

A Scalable Solution for High Energy Physics

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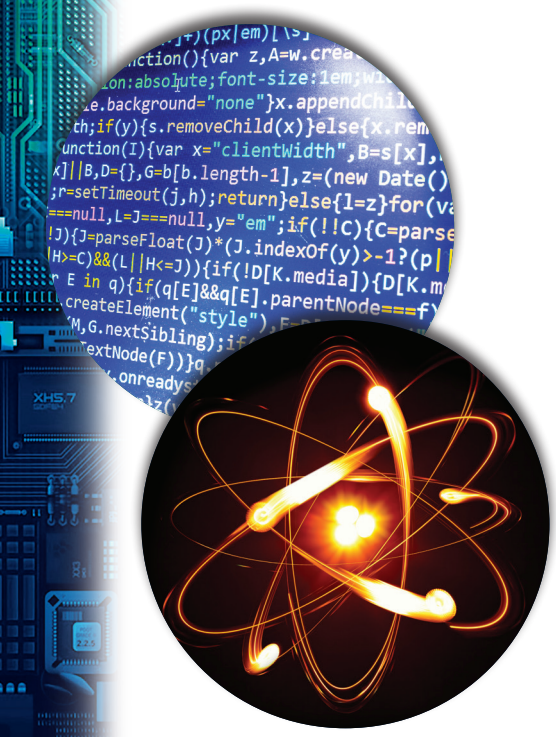


Customer Application: High Density, High Speed Acquisition for Plasma Control

A world-renowned research institute recognized a need to upgrade their plasma control system. In common with many of their counterparts in the high energy physics community, which is adopting the MicroTCA.4 architecture as a common platform for high performance embedded computing, the research team started with MicroTCA.4 as a reference for their high speed, high density data acquisition system.

They approached VadaTech with a list of innovative specifications, including very high speed and high density acquisition, with line rate data transfer to AMC725 which is an Intel based Processor AMC (PrAMC).

After a careful analysis of MicroTCA.4 boundaries and selecting the appropriate Xilinx FPGA and ADC, VadaTech designed the AMC523 and MRT523 for the MicroTCA.4 chassis.

Architecture choice:

Our R&D experts collaborated with the end-user and local technical support to agree the architecture, balancing a complex set of parameters created by the high speed and high density specifications.

The first challenge was to find the best architecture to fit as many acquisition channels as possible, without compromising analog and digital signal integrity. VadaTech selected the AD9653 from Analog Devices (Quad, 16 bit, 125 MSPS ADC), and chose to dedicate the MRT523 rear transition module (RTM) for the analog to digital

conversion. This architecture gives the designer enough space to fit three AD9653 devices on the AMC to enable a total of 12 acquisition channels and provides the best isolation between the high speed digital signals (FPGA, Fabric, etc...) and the analog signals. Having the 12 analog inputs in the rear of the chassis also made it easier to integrate the dense acquisition system in a cabinet on site.

The second challenge was to handle the data rate of 24 Gb/s generated by the 12 ADC. VadaTech selected a Kintex FPGA from Xilinx (XC7K410T: 406720 logic cells, 1540 DSP slices and 28620 Kb RAM blocks) in order to give the customer enough processing power to implement its algorithms. The high speed buffering is handled by 2 GB of DDR3 memory, with enough bandwidth and capacity to do real time buffering of 600ms of acquisition.

To support the data transfer between the FPGA and the acquisition server, VadaTech provided the customer with different high speed paths:

1. For applications with an Intel acquisition server running on a PrAMC, the customer can use the Fabric interface (lanes 4 to 11 of the backplane, up to PCIe 8x gen2). With a maximum data rate of 32 Gb/s, this path provides enough bandwidth to do real time acquisition.
2. For customers using an external acquisition server, VadaTech included 4 SFP+ connectors with a direct LVDS link to the FPGA's GTX blocks.

Our engineers added a dual MAX5878 DAC (16 bit, 250 MSPS) to the AMC523 for applications using analog outputs (control loop, calibration, tests and other...).

Physics experiments use their own high precision reference clock and trigger network. VadaTech designed a flexible clock and trigger routing on the AMC523, to cover every possible case.

The reference clock can either come from the on-board clock generator, the backplane (TCLKA, TCLKB, TCLKC or TCLKD), or the AMC523 front panel. Low jitter clocks are generated from the reference clock to drive the 3 quad ADC and the dual DAC. ADC and DAC sampling clocks can be adjusted by software, using the Si5345A configuration tool.

The acquisition trigger can also come from the backplane (TCLKA, TCLKB, TCLKC or TCLKD) or from the AMC523 front panel.

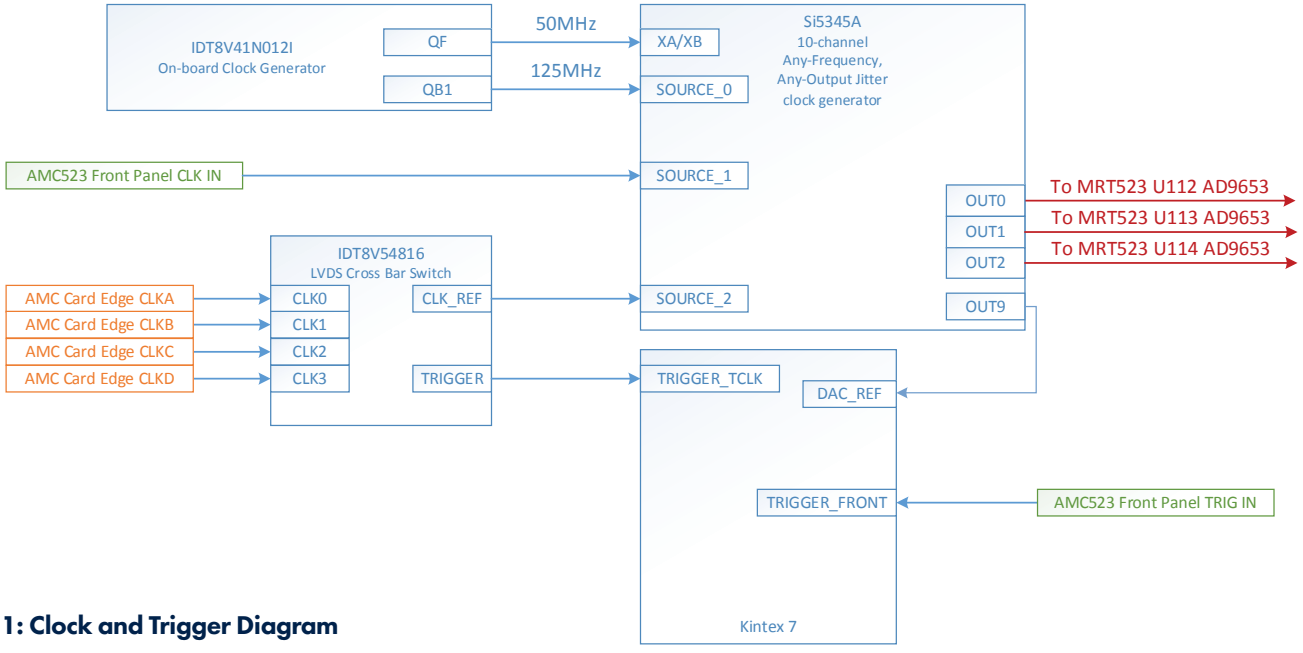
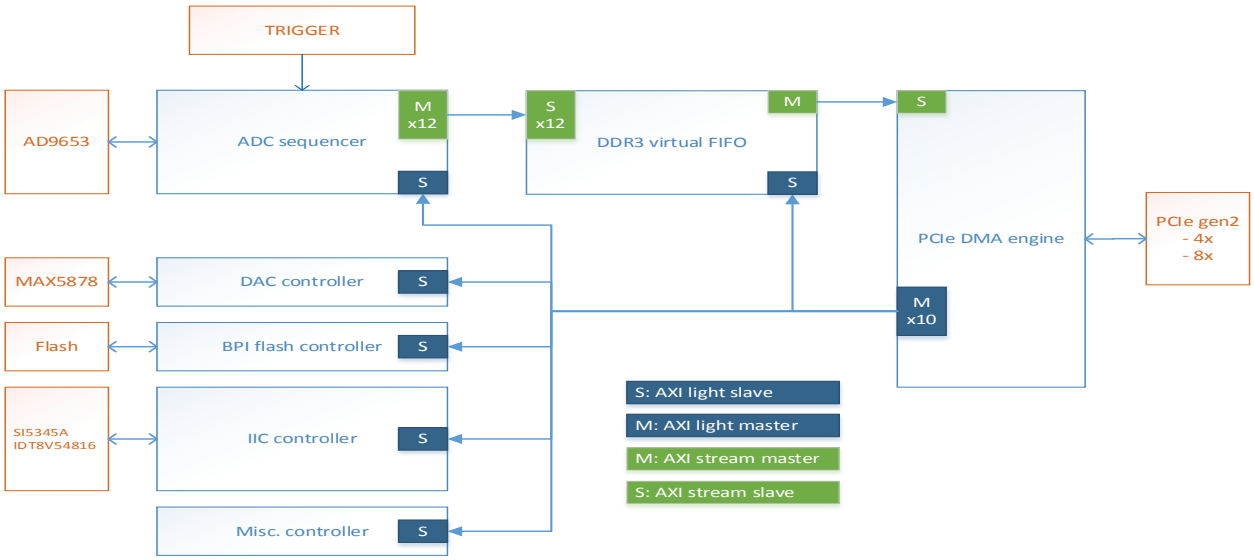


Figure 1: Clock and Trigger Diagram

Figure 2: Acquisition IP Blocks Diagram



Integration Challenge:

With high density, high speed systems, the complexity of software development can become overwhelming. Designing acquisition software with a level of performance that meets the capabilities of the hardware involves a team of engineers with a wide range of specialties. This includes expertise in signal processing, FPGA design, networking, high-performances kernel drivers and more.

Most research institutes do not have the in-house capability to provide all of these design disciplines. VadaTech's engineering team has extensive experience in complex design, and in this application the team put its expertise to work in alleviating the complexity of the hardware through a high level API. This allowed the end-user and local technical sales channel to concentrate on the development of EPICS drivers and allocate precious resources to their specific experiment tasks.

The first task on the road to high level API was to design FPGA firmware that uses the full capability of the hardware.

The IP is built around the AXI protocol, allowing a simple interconnection between VadaTech's firmware and the customer's own IP.

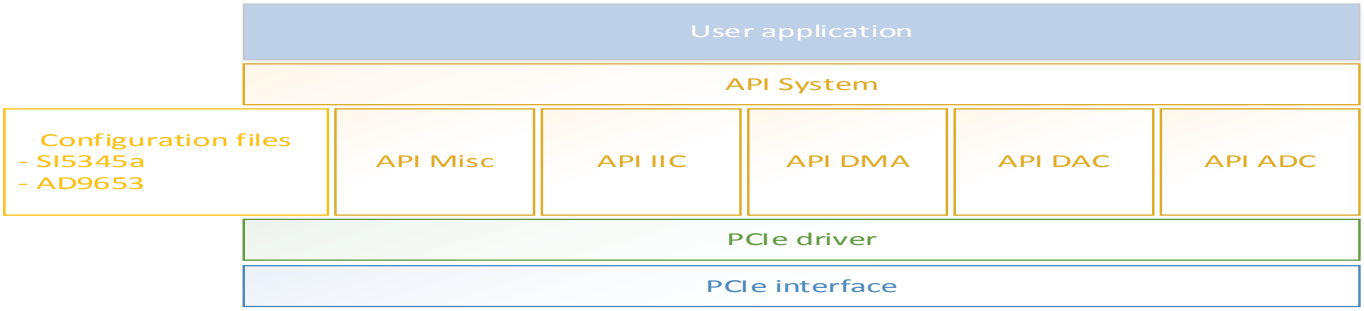
The DDR3 Virtual FIFO and the PCIe DMA engine are the main building blocks of the high speed interconnection between the FPGA and the acquisition server. The DDR3 Virtual FIFO allows the real time buffering of 1 to 12 ADC channels. The PCIe DMA engine empties the Virutal FIFO (at line rate (1.65 GB/s in PCIe 4x gen 2, 3.3 GB/s in PCIe 8x gen 2).

We added an ADC sequencer to give the user flexibility in the definition of the acquisition sequence. Each ADC channel can be activated or deactivated. The acquisition mode can be one the following:

- Single snapshot (start on trigger for a defined period of time)
- Repetitive snapshots (start on trigger for a defined period of time, stop acquisition for a defined period of time, start acquisition...)
- Free running (start on trigger for an unlimited period)

These 3 modes cover the requirements for most experiments. The association of an external reference clock and trigger, a cycle-accurate versatile sequencer and 64 bit samples' time-stamping make it possible to create complex experiments with an array of synchronous sensors with low jitter.

Figure 3: Layers providing easier control of the platform by the end-user



We designed a high level API to run on the server side.

This API is built with 3 layers, each layer with a decreasing level of complexity. This architecture gives users total control over the level of detail they need in their application. Our engineers took care at each level to guarantee the lowest overhead possible.

VadaTech used its "Zero Copy" DMA IP with a fixed buffer allocation strategy for the PCIe driver in order to reduce the API overhead close to zero. The result is that the FPGAs write directly in the user application's buffers without any processing needed from the driver. The system API hides the complexity of this setup by providing a set of very high-level functions and example code.

This high performance design lets the user focus on its own algorithms, and provides assurance that most of the server's CPU time is available for its own processing.

As this API is mainly designed for the scientific community, care was taken to assure the compatibility with the main scientific Linux distribution, SL /MRGR. Scientific Linux and Real Time MRG (Red Hat) are supported on the VadaTech AMC72X Intel PrAMC series.

Security – High Density - Integration choice:

The VT812 chassis offers security with redundancy capabilities at both MCH and power module levels. This allows failover and hot-swap capability in case of failure.

Rear I/O connections provide secure cable management and easy access to instruments,

Figure 4: Dual 500W/800W redundant power modules

improving the safety of the installation/maintenance team in critical environment. The choice of SSMC connectors allows the 12 ADC and 2 DAC I/O to be available via the same rear panel.

The 2U VT812 chassis platform provides a hybrid of the MTCA.4 (4 slots) and MTCA.0 (4 slots) standards. The chassis solution provided the end-user with the ability to add a significant amount of storage. In some installations, the data acquisition is linked to a separated storage rack accessible for analysis. This chassis allows the user to select between connecting to a distant storage rack and local storage in the chassis accessible for off-line analysis.

VadaTech manufactures six different chassis compatible with MTCA.4 specifications. VT816 1U chassis is an excellent choice for more compact acquisition platforms that don't require higher slot options and redundancy. The chassis platform holds dual AMCs and the corresponding RTMs per MTCA.4. It has an integrated MCH, Intel Xeon E3 v2 processor and optional single/dual SSD drive for a complete integrated solution. The chassis routes PCIe Gen 3 x8 to each AMC slot providing four

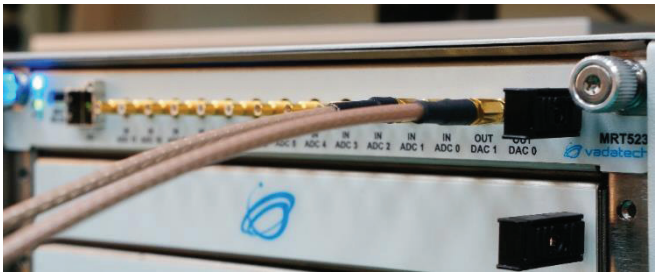


Figure 5: MRT523 SSMC connectors and SFP+ expansion

times the bandwidth available in the VT812. See Figure 6 for an image of the VT816.

With more than 300 products in ATCA and MicroTCA architecture, VadaTech has a strong experience in building cutting edge solutions to solve customers' most challenging business problems.

Figure 6: VT816, 1U µTCA.4 Chassis with 2 AMC Slots, PCIe Gen 3