Solution Brief

Robust FPGA module design with up to 150W and 500Gbps data stream capability

VadaTech customers are constantly innovating, developing the next generation of data processing devices that take advantage of the most adaptable silicon available.

VadaTech's selection of the largest FPGA models from the Xilinx Virtex® UltraScale+™ family has provided our system integrators with new horizons to expand their application data processing capability.

This comes with a challenge for VadaTech, to push forward the capabilities of existing open standards, and to support higher power and cooling requirements as well as signal integrity for a growing number of high-density high-speed SERDES interfaces.

This solution brief summarizes the challenges, the new boundaries explored, and the innovations released by VadaTech to the benefit of our demanding customers.

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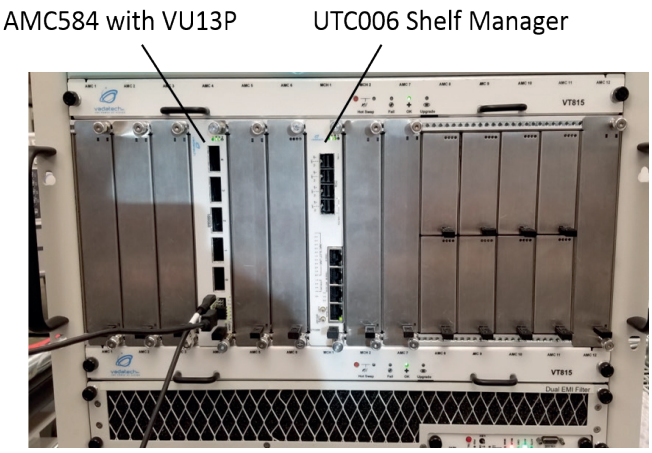
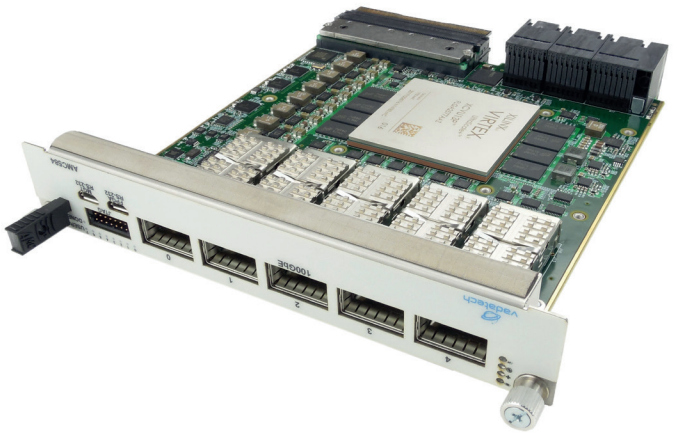
Platform Configuration

The XCVU13P is embedded in the AMC584 standard module which is installed in a 19" VT815 chassis. Two different FPGA test images have been generated by our software team, in coordination with Xilinx, in order to generate ~95W and ~150W on the AMC584 by implementing intense FPGA processing, to support integration test. Once the FPGA is loaded, we can activate the processing and monitor the power consumption as well as the onboard temperature stability. Adding a neighboring module linked over the RTM we are able to also check the signal integrity with PRBS31 tests to confirm the SERDES links at up to 25Gbps/lane.



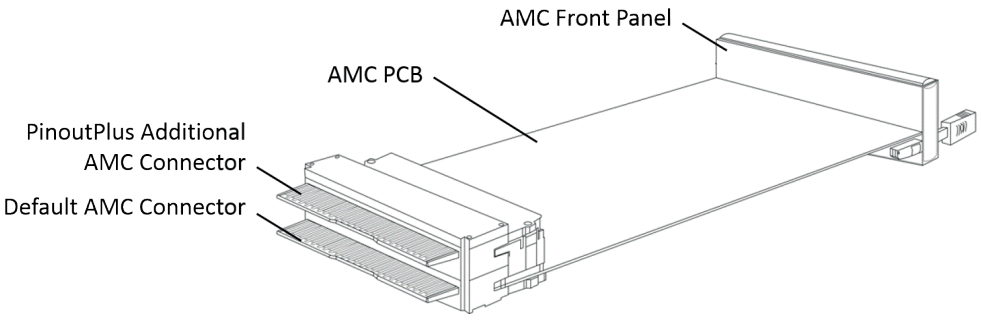
The VT815 shown above is the only chassis on the market providing over 3kW power supply to 12 slots compatible with standard and PinoutPlus modules, and with capability to provide enough airflow to guarantee the temperature stability of AMC584 in a 150W configuration.



AMC584 shown on the left is a FPGA processing module with XCVU13P providing dual 550Gbps bandwidth to neighboring modules via Zone 3 connection and 5x 100Gbps interface to the network via front panel expansion. The UTC006 shown on the right includes the Management Controller for the Power Modules, Cooling Units, and up to 12 AMCs within the chassis. It also manages the fabric switch (Fabric options include PCIe Gen3, 10/40GbE, Xilinx Virtex-7 FPGA, Cross Bar Switch, and SRIO) as well as the standard GbE with 10GbE uplink Base Channel switch.

Power Management Challenge and PinoutPlus

In order to extend the capability of the power allocation to a standard module, VadaTech designers have implemented a second connector between the module and the backplane. VadaTech calls this configuration "PinoutPlus". The VT815 implements "PinoutPlus" and provides dual backplane connectors to each slot. This second tongue connector is permissible within the MicroTCA standards and is implemented using widely available components, so this hardware approach can be used by other vendors in the market. As a result, the AMC584 is able to draw more current (up to 15A) from the chassis power module. We show below a simple PinoutPlus diagram, and 12.6A drawn by the AMC584 in AMC slot 6 of the VT815 with the 150W image:



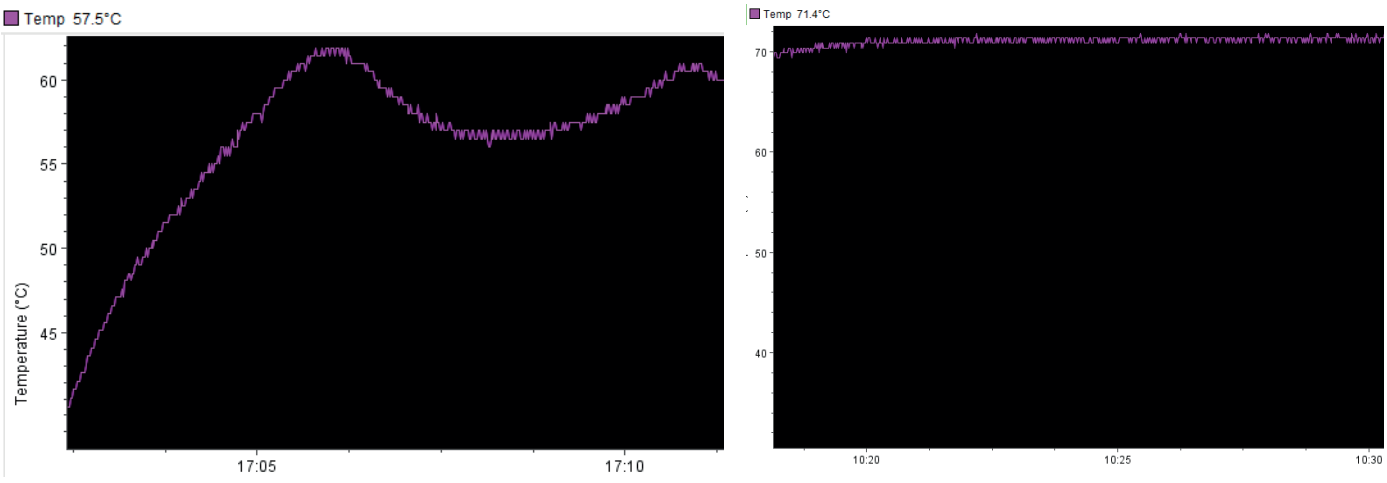
PinoutPlus Diagram on a standard AMC single-width module

```
Load Power Status
                          Management      Payload         Payload     Payload
Module     Present        Power to Load   Power to Load   Draw        Required
                                                          in Amps     in Amps
------     ------         -------------   -------------   -------     --------
MCH1       No             --------        --------        -----       -----
MCH2       Yes            Good            Good            3.4         *5.5
CU1        Yes            Good            Good            3.3         *10.0
CU2        Yes            Good            Good            3.6         *10.0
AMC6       Yes            Good            Good            12.6        *15.0
```

The VT815 power module status reports a current consumption of 12.6A out of the 15A allocated by the UTC006 controller to the AMC584 used in the slot AMC6 (151.2W).

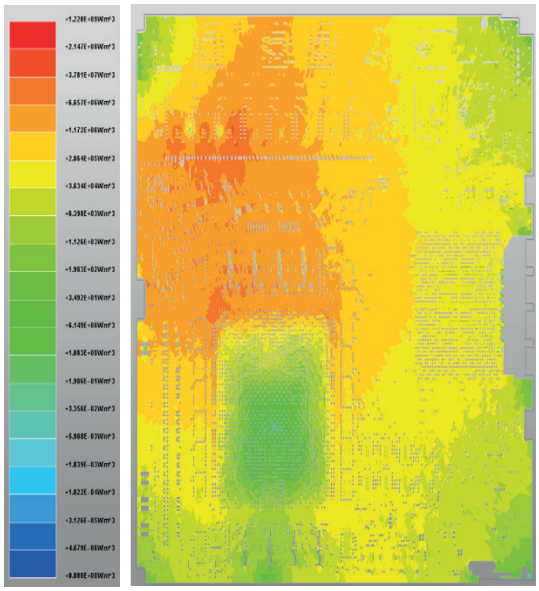
Temperature Stability and Monitoring

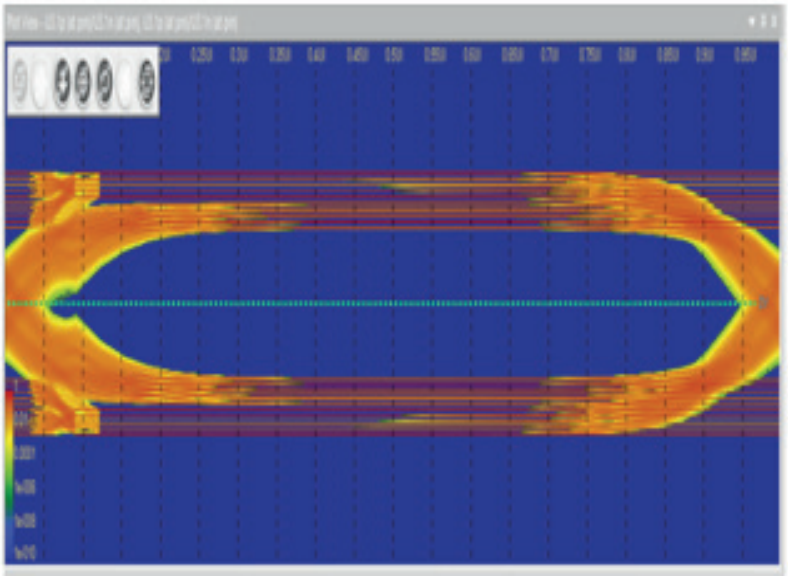
The user can monitor in real time the stability of the onboard temperature using the command lines available in the UTC006 controller or the graphic user interface, below are examples of the AMC584 onboard temperature of the AMC584 with the 96W (stable at ~60 degC) and 150W (stable at ~70degC) FPGA images:



Signal and Power Integrity Challenge

Simulation tools and tight control over PCB fab process, including specific stackup and backdrill techniques, are essential to guarantee the Signal Integrity (SI) of high speed SERDES and the Power Integrity (PI) in such a high-density module. VadaTech simulation set of tools includes 2D analysis and 3D electromagnetic field simulator for RF Design. Below on the left is an example of PI simulations to accurately model power delivery network and noise propagation on PCBs. Below on the right is an example of a Tx channel passed eye mask SI analysis in a 100G design. Both simulations have been performed at VadaTech.





The AMC584 provides dual 550Gbps bandwidth to the neighboring cards via the RTM connector and additional 5x 100Gbps via the front panel QSFP28. VadaTech performs 100% in-house design verification and automated tests. We show below the PRBS31 error free data speed test respectively at 28Gbps on the first 10 of 44 SERDES routed to the Rear Transition Module and at 25Gbps on one of the five 100G front expansion consisting of 4 SERDES:

192.168.106.6 - Remote Desktop Connection

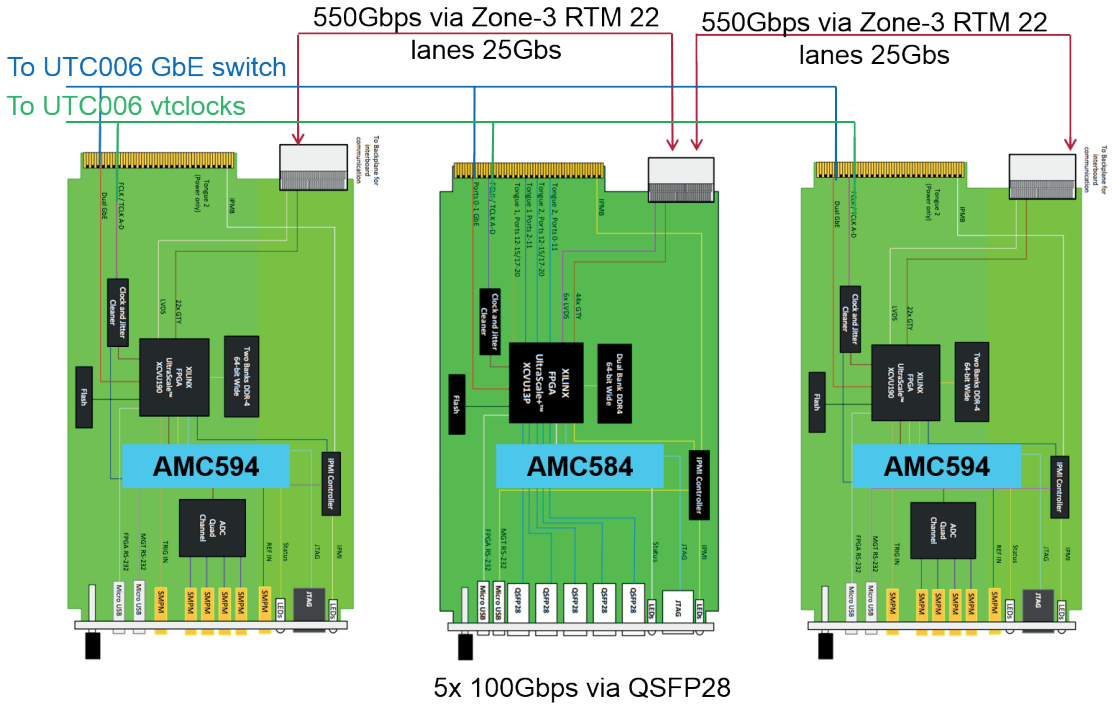
Serial I/O Links

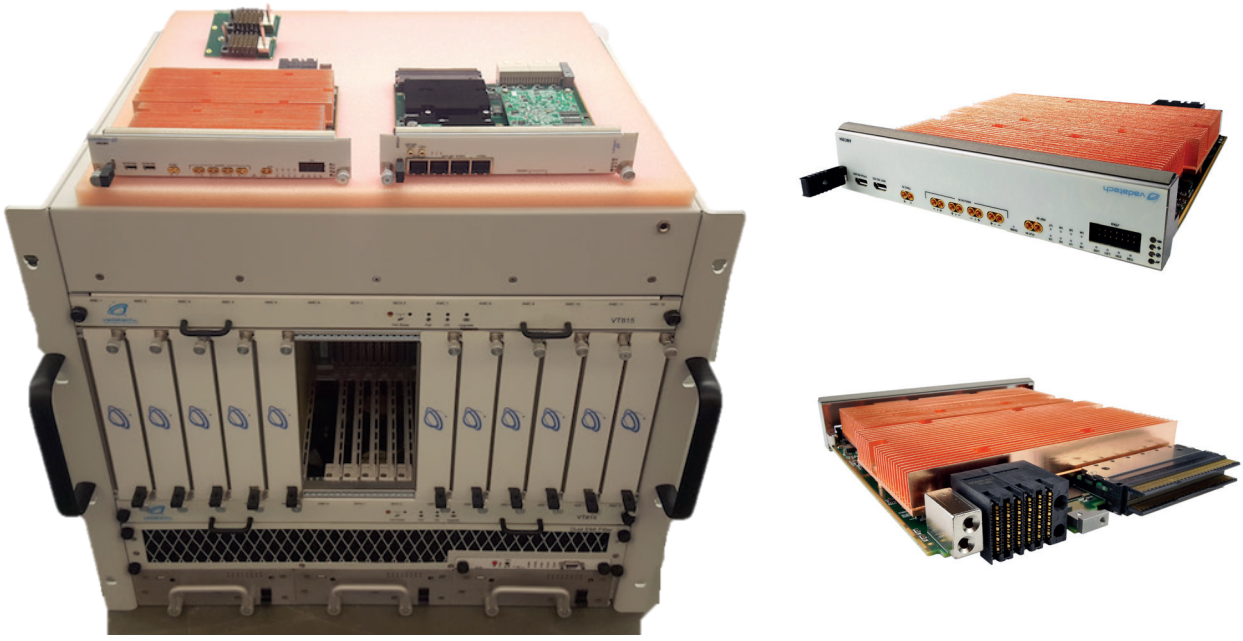
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor
Ungrouped Links (0)											
Link Group 0 (44)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 20	MGT_X0Y32/TX	MGT_X0Y32/RX	28.124 Gbps	2.864E13	0E0	3.491E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 21	MGT_X0Y33/TX	MGT_X0Y33/RX	28.124 Gbps	2.864E13	0E0	3.491E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 22	MGT_X0Y34/TX	MGT_X0Y34/RX	28.120 Gbps	2.864E13	0E0	3.491E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 23	MGT_X0Y35/TX	MGT_X0Y35/RX	28.124 Gbps	2.864E13	0E0	3.491E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 24	MGT_X0Y36/TX	MGT_X0Y36/RX	28.138 Gbps	2.864E13	0E0	3.492E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 25	MGT_X0Y37/TX	MGT_X0Y37/RX	28.124 Gbps	2.864E13	0E0	3.492E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 26	MGT_X0Y38/TX	MGT_X0Y38/RX	28.124 Gbps	2.864E13	0E0	3.492E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 27	MGT_X0Y39/TX	MGT_X0Y39/RX	28.130 Gbps	2.864E13	0E0	3.492E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 28	MGT_X0Y40/TX	MGT_X0Y40/RX	28.124 Gbps	2.864E13	0E0	3.492E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 29	MGT_X0Y41/TX	MGT_X0Y41/RX	28.120 Gbps	2.864E13	0E0	3.492E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)
Link 30	MGT_X0Y42/TX	MGT_X0Y42/RX	28.124 Gbps	2.864E13	0E0	3.492E-14	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor
Link Group 1 (4)							Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	4.08 dB (0111
Link 20	MGT_X0Y8/TX	MGT_X0Y8/RX	25.782 Gbps	9.921E11	0E0	1.008E...	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	4.08 dB (0111
Link 21	MGT_X0Y9/TX	MGT_X0Y9/RX	25.782 Gbps	9.921E11	0E0	1.008E...	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	4.08 dB (0111
Link 22	MGT_X0Y10/TX	MGT_X0Y10/RX	25.782 Gbps	9.922E11	0E0	1.008E...	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	4.08 dB (0111
Link 23	MGT_X0Y11/TX	MGT_X0Y11/RX	25.782 Gbps	9.922E11	0E0	1.008E...	Reset	PRBS 31-bit	PRBS 31-bit	1.16 dB (00101)	4.08 dB (0111

Dual 56Gbps Converter and Processing for Telecom

In this application our customer used a high-end 56Gbps ADC embedded in AMC594 together with a Xilinx Virtex UltraScale XCVU190 for the development of their next generation of modulation in a Telecom application. The AMC594 has 22 SERDES routed to a high-speed RTM connector. The AMC584 has 44 lanes routed to the high-speed RTM allowing up to two AMC594 to be integrated with a single AMC584 for post processing as shown in the diagram below:





The VT815 with the Dual 56Gbps ADC w. Virtex UltraScale module AMC594, UTC006 switch and management controller, and rear high-speed module. Rear view of the AMC594 shows the high-speed RTM w. 22x 25Gbps capability and the PinoutPlus connector.

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