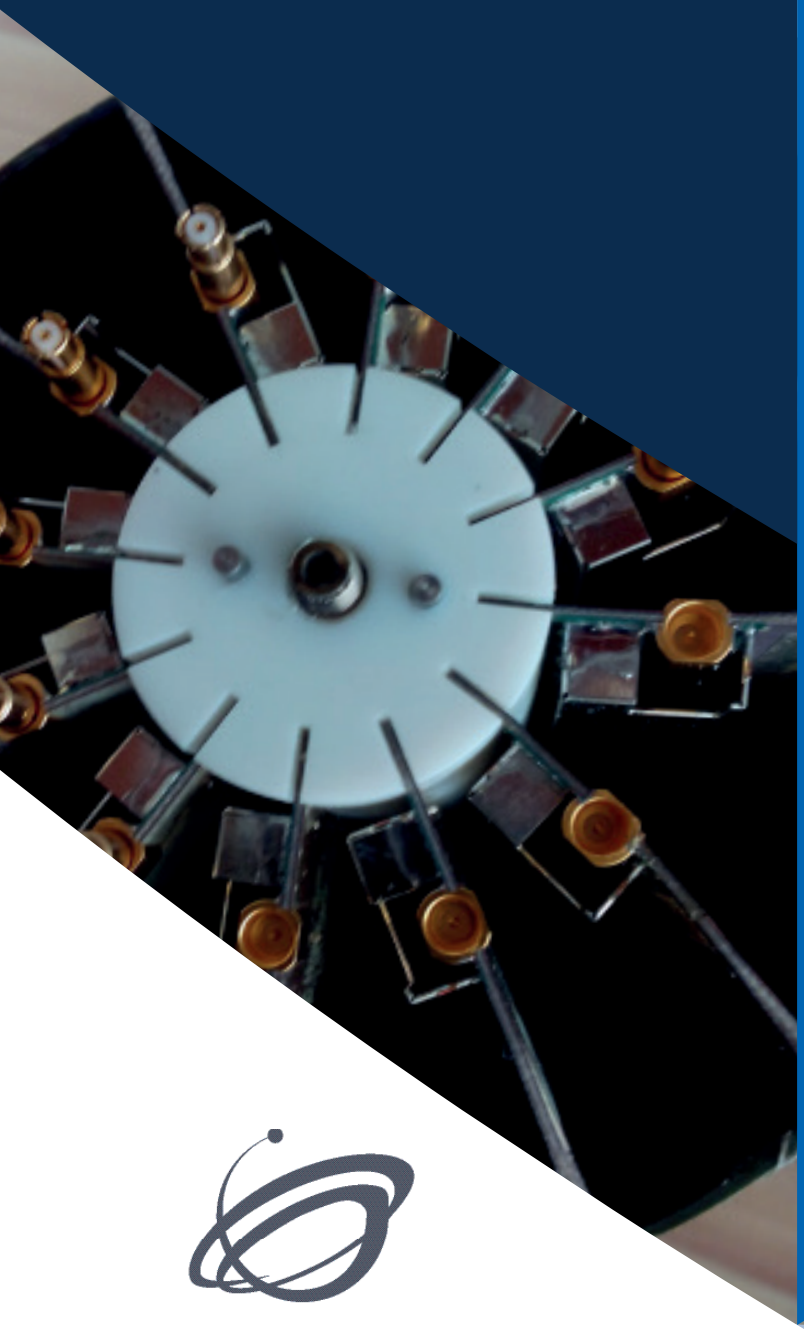
Solution Brief

Dual ADRV9009 phase-synchronized on scalable FMC 239



With an open-standard product line based on Analog Devices ADRV9009 highly integrated RF transceiver and Xilinx Zynq Ultrascale+ FPGA family, VadaTech provides the most powerful and versatile platform to develop and deploy the next generation of:

- simultaneous 2G, 3G, 4G and 5G base station
- massive MIMO
- phased array radar & beam forming
- SIGINT

These applications usually require phase synchronization between the TX channels and between the RX channels and a system level antenna calibration is performed to equalize the phase difference across channels. This calibration can become very complex and time consuming if the phase difference across channel is unpredictable over each system reboot.

TThe FMC239 can be implemented across multiple ADRV9009 transceivers, which is the synchronization mechanism to allow the user to set the phase of the transceiver's LO and JESD link latency to a deterministic value across reboot. With this synchronization, all ADRV9009 in the system start in a predictable condition. As a result, the system level calibration is simplified and needs to be run less often.

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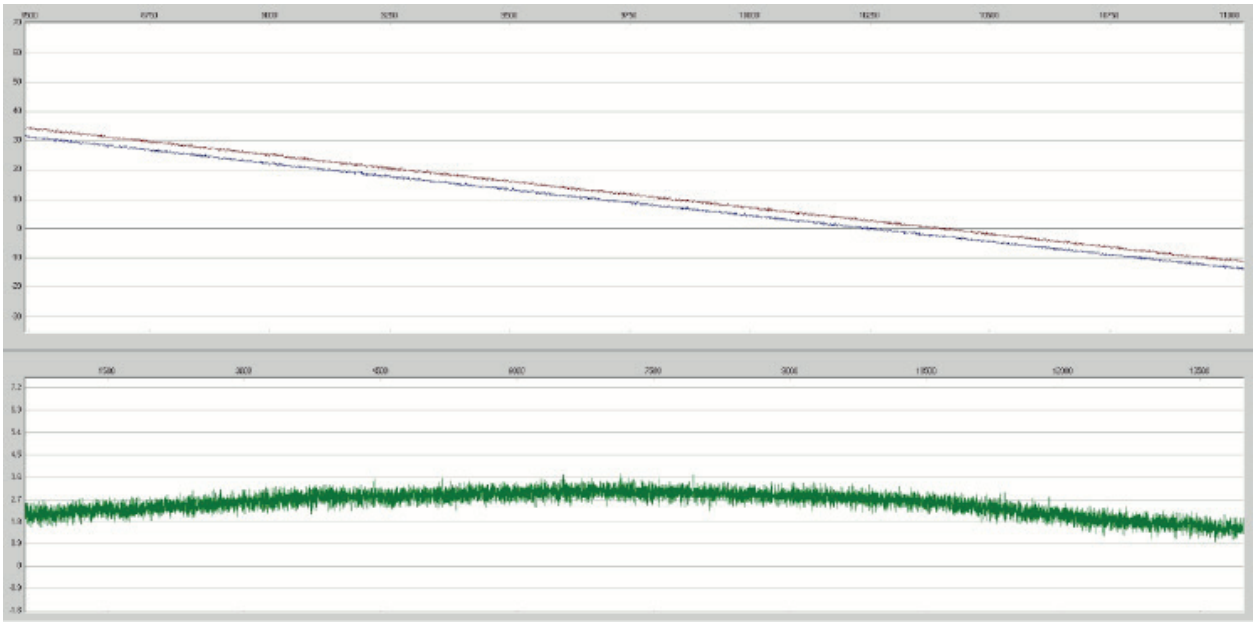
Rx synchronization

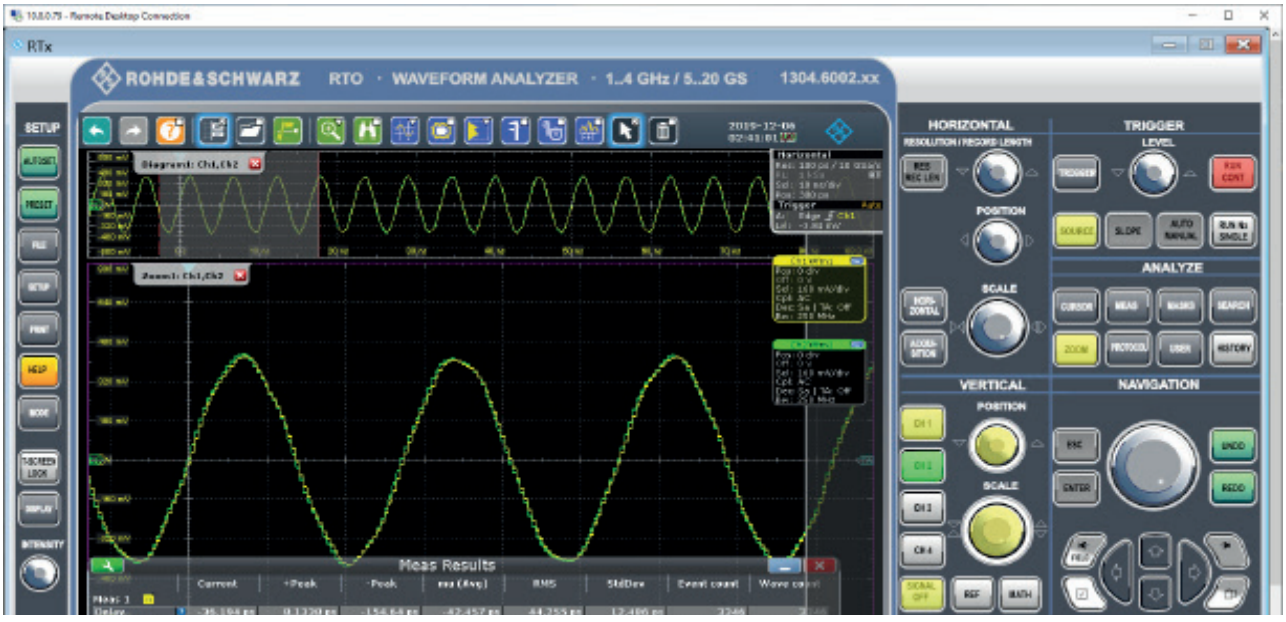
For this test we have the external 100MHz as a clock reference for the FMC239 and we connect one -15dBm sine wave of 199.99MHz at the input of RX1/0 and RX1/1 (respectively from ADRV9009/0 and ADRV9009/1 of FMC239). We then proceed to perform a snapshot acquisition and download the data.

The phase difference between the two snapshots is measured using Analog Devices Visual Analog tool. The phase difference between the two snapshots is measured between 1.9 and 3.5 degrees at room temperature.



Tx synchronization

For this test, we connect the external 100MHz reference clock to the FMC239 front panel clock input and measure TX1/0 and TX1/1 (respectively from ADRV9009/0 and ADRV9009/1 of FMC239) with the oscilloscope. The ADRV9009 LO is set at 200MHz. We generate a sine wave on both ADRV9009 TX at 180MHz and measure the delay between the two outputs on the RTO 1044 oscilloscope. We measure an average of -42ps delay, with a standard deviation of 12ps between the outputs. That represents a delay of 2.7 degrees and a standard deviation inferior to 1 degree at this frequency at room temperature.



Scalability

Systems which are not modular are hard to maintain or extend. The VPX and TCA are modular architectures like VME, cPCI and others. There is a standard specification (Mechanical, Electrical and Environmental) which enables a chassis slot configuration where one slot can be used with the whole ecosystem of modules such as an FPGA Carrier, DSP, CPU, I/O or network expansion card. This allows a user to scale up or down a system without having to redesign it entirely like in a non-standard custom design.

Interoperability

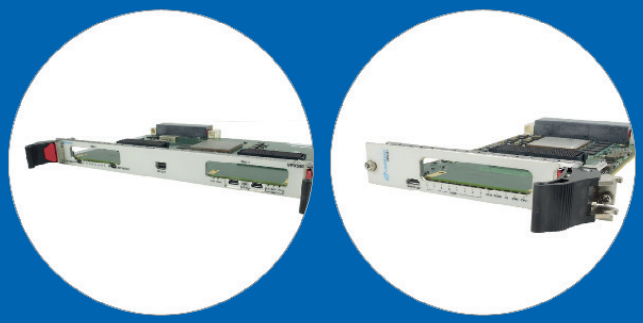
The US Department of Defense and other actors in the Industry are mandating improved implementation of open standards and interoperability. VPX (VITA) and FMC (PICMG) specifications have been focused at the board level, but there is also a need for considering system-level requirements to improve interoperability and reduce customization, testing, cost, and risk.

As a result, the OpenVPX (VITA) and TCA (PICMG) aim at defining some pinouts and interoperability points. "Open" means that the interfaces are completely documented and accessible within the community of interest, and can be implemented by different organizations without royalties.

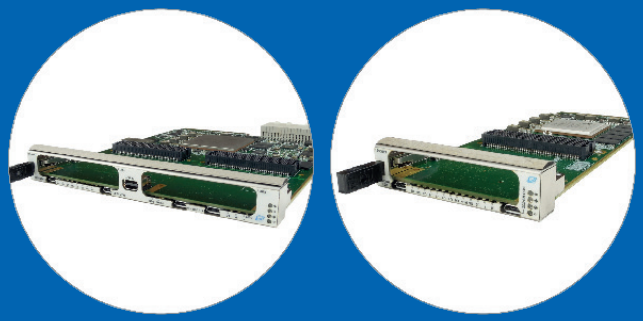
Open standards are developed by standard organizations that have hundreds of members with an extremely diverse technical talent base. Interoperability eliminates vendor lock-in unlike in a non-standard custom design.

Affordability

The specifications of systems are generally too sophisticated to be fully designed or developed by individuals or one small team and end up be shared across multiple teams (and manufacturers). Without a strong common open-standard specification, the understanding of each manufacturer and their teams is the projection of the truth onto each individual's "basis set" of pre-dispositions, talents, and experience, leading to costly misinterpretations. Open Standards are specifically created to define ground rules and reduce life-cycle costs.



OpenVPX FPGA Carrier for VITA standard FMC+
XCZU19EG on VPX580 with double FMC+ sites (left)
XCZU15EG on VPX581 with single FMC+ site (right)



Standard TCA FPGA Carrier for VITA standard FMC
XCZU19EG on AMC580 with double FMC sites (left)
XCZU15EG on AMC581 with single FMC site (right)

PCIe FPGA Carrier for VITA standard FMC
XCKU115 on PCI592 with single FMC site

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